SYSTEM

User Guide

PC1-GROOVE • ***CompactPCI*** ® PlusIO
Core™ i7 Processor High Performance CPU Card

Suitable for Classic CompactPCI© and PICMG 2.30 CompactPCI® PlusIO Systems

Document No. 5713 • Edition 27 • 1 October 2015

PC1-GROOVE

Contents

About this Manual

This manual describes the technical aspects of the PC1-GROOVE, required for installation and system integration. It is intended for the experienced user only.

Edition History

Ed.	Contents/*Changes*	Author	Date
1	User Manual PC1-GROOVE, english, initial edition (Text #5713, File: pc1_uge.wpd)	gn	2010-03-22
2	Added photos, added relational links	jj	20 May 2010
3	Part # change USB connector	jj	19 October 2010
4	Added to table Feature Summary: +3.3V V(I/O) option	jj	5 November 2010
5	Changed default setting of switch DSW1	gn	2011-02-24
6	Changes due to Revision 1	gn	2011-03-31
7	Added description of the front panel handle integrated switch	gn	2011-04-13
8	Added photos showing how to force system shutdown using the front panel handle integrated switch	jj	12 May 2011
9	Added photos 'Small Systems' and 'Rugged Systems'	jj	13 May 2011
10	BIOS usage of GP LED - document link added	jj	18 May 2011
11	Added photos 'Hybrid Systems', added photos of mezzanine modules and side cards, added photos of rear I/O module	jj	24 May 2011
12	Added factory settings of switch DSW1 for different side boards	gn	2011-06-09
13	Added Power Requirements	gn	2011-06-17
14	Added PCI-ID of JMB362 Rev. C Controller	gn	2011-06-30
15	Table Feature Summary: Added Clock Rates of CPU Graphics Core	jj	26 July 2011
16	Added photo PC1-C47 assembly	jj	16 August 2011
17	Added photo C47-MSATA mezzanine module	jj	22 August 2011
18	Added photos front view	jj	25 August 2011
19	Added photos DisplayPort adapter, front panel handle micro switch	jj	2 September 2011
20	Added photos DisplayPort cable adapter DVI & VGA	jj	19 January 2012
21	Added photos low profile mezzanine modules exploded view	jj	28 March 2012
22	Added MTBF value to table Feature Summary	gn	2012-05-04
23	Added recommendation regarding DsiplayPort cable (pin 20 issue)	jj	5 March 2013
24	Added information regarding selection of suitable intermediate PCB for mezzanine connector SDVO2	jj	3 April 2013
25	Added photos PC1-PCS assemblyies	jj	29 April 2013
26	Clarified resetting of UEFI BIOS settings to factory defaults	gn	2015-01-16
27	Added photos C48-M2 low profile mezzanine storage module	jj	21 May 2015
28	Table 'Feature Summary' - added RTOS support	jj	1 October 2015

Related Documents

Related Information PC1-GROOVE	
PC1-GROOVE Home	www.ekf.com/p/pc1/pc1.html
PC1-GROOVE Ordering Information	www.ekf.com/p/pc1/pc1_pie.pdf

Nomenclature

Signal names used herein with an attached '#' designate active low lines.

Trade Marks

Some terms used herein are property of their respective owners, e.g.

- Pentium, Celeron, Core™ i7, Arrandale, Ibex Peak-M, Calpella Platform, iAMT, Hanksville, Hartwell: ® Intel
- CompactPCI : ® PICMG
- Windows XP, Windows 7, Windows 8: ® Microsoft
- EKF, ekf system: ® EKF

EKF does not claim this list to be complete.

Legal Disclaimer - Liability Exclusion

This manual has been edited as carefully as possible. We apologize for any potential mistake. Information provided herein is designated exclusively to the proficient user (system integrator, engineer). EKF can accept no responsibility for any damage caused by the use of this manual.

Standards

Theme	Document Title	Origin
CompactFlash	CF+ and CompactFlash Specification Revision 3.0	www.compactflash.org
CompactPCI	CompactPCI Specification, PICMG 2.0 R3.0, Oct. 1, 1999	www.picmg.org
CompactPCI PlusIO	CompactPCI PlusIO Specification, PICMG 2.30 R1.0, November 11, 2009	www.picmg.org
CompactPCI Serial	Under developement	www.picmg.org
DisplayPort	VESA DisplayPort Standard Version 1.1 March 19, 2007	www.vesa.org
DVI	Digital Visual Interface Rev. 1.0 Digital Display Working Group	www.ddwg.org
Ethernet	IEEE Std 802.3, 2000 Edition	standards.ieee.org
HD Audio	High Definition Audio Specification Rev.1.0	www.intel.com/design/chipsets/hdaudio.htm
PCI Express	PCI Express® Base Specification 1.1	www.pcisig.com
PCI Local Bus	PCI 2.2/2.3/3.0 Standards PCI SIG	www.pcisig.com
SATA	Serial ATA 2.5/2.6 Specification	www.sata-io.org
TPM	Trusted Platform Module 1.2	https://www.trustedcomputinggroup.org
USB	Universal Serial Bus Specification	www.usb.org

8HP Assembly PC1-GROOVE - PCS-BALLET - C48-M2

PC1-GROOVE Features

Feature Summary

Feature Summary PC1-GROOVE	
Form Factor	Single size *CompactPCI*® style Eurocard (160x100mm²), front panel width 4HP (20.3mm)
Processor	Designed for Intel® Core™ i7 processors (codename Arrandale) with integrated graphics and memory controller ▸ Maximum junction temperature of processor core 105°C (graphics core 100°C) ▸ Enhanced Intel® Speedstep® Technology ▸ Intel® Turbo Boost Technology ▸ Dual Core Multiprocessing ▸ Intel® Virtualization Technology (VT) ▸ Intel® 64 Architecture ▸ Refresh of 5th generation graphics core with 12 Execution Units Available processors: ▸ Core™ i7-610E • 2.53GHz • 4MB L3 Cache • 35W TDP • 500/766MHz Graphics ▸ Core™ i7-620LE • 2.00GHz • 4MB L3 Cache • 25W TDP • 266/566MHz Graphics ▸ Core™ i7-660UE • 1.33GHz • 4MB L3 Cache • 18W TDP • 166/500MHz Graphics ▸ Core™ i7-620UE • 1.06GHz • 4MB L3 Cache • 18W TDP • 166/500MHz Graphics
Chipset	Mobile Intel® 5 Series Chipset (Codename Ibex Peak): QM57 Express Chipset Platform Controller Hub (PCH) with ▸ 8 PCI Express root ports at 2.5Gbps ▸ 6 x SATA 3Gbps ▸ Intel® Matrix Storage Technology (RAID 0, 1, 5, 10) ▸ High Definition Audio ▸ 14 x USB (2 EHCI controllers) ▸ Integrated GbE MAC ▸ iAMT ▸ Unified SPI Flash support ▸ 3 Digital Display Interfaces (DisplayPort, SDVO, HDMI) ▸ VGA interface with integrated 350MHz RAMDAC (resolution up to 2048x1536x24@75Hz)
Memory (RAM)	▸ Maximum memory capacity of 8GB DDR3 up to 1066MHz ▸ 512Mb, 1Gb, 2Gb, [4Gb] technologies for x8 and x16 devices ▸ Channel 0 populated as directly soldered DDR3 devices (Memory Down) ▸ Channel 1 provided as 204-pin SODIMM socket to carry DDR3 module PC3-8500 ▸ Dual channel symmetric – memory addresses interleaved for increased performance (SODIMM module size must match Memory Down size) ▸ Intel® Flex Memory Technology (dual channel interleaved mode with unequal memory population) - memory sizes maybe unequal in both the channels ▸ Dual channel asymmetric – memory sizes may differ, including no memory module populated in the SODIMM socket (single-channel)
Video	▸ Concurrently operation of two monitors with resolutions up to 2560x1536 pixel 16M colours @60Hz refresh rate (DisplayPort), up to 1600 x 1200 pixel 16M colours @60Hz (DVI-D on side boards like CCO-CONCERT) ▸ Dual screen capable (one display attached to the front panel DisplayPort connector, the other to a digital display interface provided by a side board) ▸ Front panel option: D-Sub (female HD15) VGA connector available, replaces DisplayPort connector ▸ Mezzanine option: Secondary DVI-D connector at mezzanine card front panel allows for dual digital flat panel operation, suitable mezzanine modules e.g. CCH-MARIACHI, CCI-RAP, CCJ-RHYTHM, CCO-CONCERT. Side boards providing a 2nd DisplayPort are projected

Feature Summary PC1-GROOVE	
USB	▸ All ports over-current protected, data transfer rate of up to 480Mbps, conforming to USB2.0 ▸ 2 x USB type A connector (front panel) ▸ 4 x USB ports J2/P2 PlusIO ▸ 2 x USB ports via J-EXP expansion interface option (in use by several mezzanine side boards) ▸ 4 x USB ports via J-HSE (e.g. C40-SCFA mezzanine storage module) ▸ Dual EHCI controllers provided by PCH QM57
Ethernet	▸ Total of four 10/100/1000Mbps Gigabit Ethernet controllers, two accessible via RJ45 jacks from the front panel, two fed to J2/P2 PlusIO ▸ ETH1 equipped with Intel® 82577LM PHY (codename Hanksville), serves also as AMT out of band communication path (MAC provided by PCH QM57), Jumbo Frame support up to 4KB ▸ ETH2…4 equipped with Intel® 82574L GbE controller (codename Hartwell), connected to local PCIe lanes, supports 9KB jumbo packets, TimeSync Offload compliant with 802.1as specification
SATA	▸ Total of eight 3Gbps SATA channels available ▸ Quad-channel Serial ATA 3Gbps available for J2/P2 PluIO (derived from PCH QM57) ▸ Intel® Matrix Storage Technology MST (Raid 1, 0, Matrix Raid) ▸ Secondary on-board PCIe to SATA controller JMB362, dual channel SATA RAID, available via J-HSE expansion connector (plus 2 SATA channels in addition from PCH QM57) ▸ Additional PCIe to SATA controller on mezzanine side boards e.g. CCI-RAP, CCK-MARIMBA, CCL-CAPELLA, CCO-CONCERT
PATA (IDE)	▸ Option mezzanine module attached to J-HSE expansion connector ▸ C40-SCFA mezzanine module available with on-board SATA to PATA bridge and CompactFlash socket
PCI Express	▸ 12-Port PCIe Gen 2 switch provides 4 lanes to PCIe high-speed connector J-PCIE for CCJ-RHYTHM and other mezzanine expansion cards, and 4 lanes to J2/P2 PlusIO interface ▸ Possible configurations on each interface 1 Link x 4 Lanes, 4 Links x 1 Lane

Mezzanine Side Board I/O	▸ J-EXP Legacy expansion interface connector LPC/USB/Audio (SIO, USB, HD Audio)
	▸ J-HSE High-speed expansion interface connector (4 x SATA, 4 x USB)
	▸ J-PCIE PCI Express 4-lane high-speed expansion connector
	▸ J-SDVO2 additional digital graphics port high-speed expansion connector
	▸ Suitable mezzanine companion side boards available, e.g.:
	  ▸ *CCI-RAP*: 2 x PCI Express Mini Card sockets (WLAN, GSM, Wimax, Intel® Turbo Memory), options secondary DVI-D, IEEE 1394 (FireWire), USB SSD, C20-SATA mezzanine storage module (accommodates up to 2 SATA hard disk drives 2.5-inch RAID capable)
	  ▸ *CCJ-RHYTHM*: CompactPCI Express system slot controller function by on board 6-port 24-lane PCIe switch, options DVI-D, IEEE 1394 (FireWire)
	  ▸ *CCK-MARIMBA*: PMC/XMC module carrier, option C20-SATA mezzanine storage module
	  ▸ *CCL-CAPELLA*: Up to 4 Gigabit Ethernet ports, options IEEE 1394 (FireWire), USB SSD, C20-SATA mezzanine module
	  ▸ *CCO-CONCERT*: Audio analog/digital, option secondary DVI-D
	  ▸ *C23-SATA*: PCIe to 2 x SATA 1 x PATA controller
	  ▸ *C40-SCFA*: SATA to PATA bridge & CompactFlash header, option USB SSD, 4HP envelope maintained
	  ▸ *C42-SATA*: 1.8-inch SATA Solid State Drive (SSD), 4HP envelope maintained

J2 *CompactPCI*® *PlusIO*	▸ Suitable PlusIO backplanes available (e.g. Schroff) ▸ High-Speed UHM connector ▸ 4 x PCIe ▸ 4 x Serial ATA (SATA) ▸ 2 x Gbit Ethernet ▸ 4 x USB

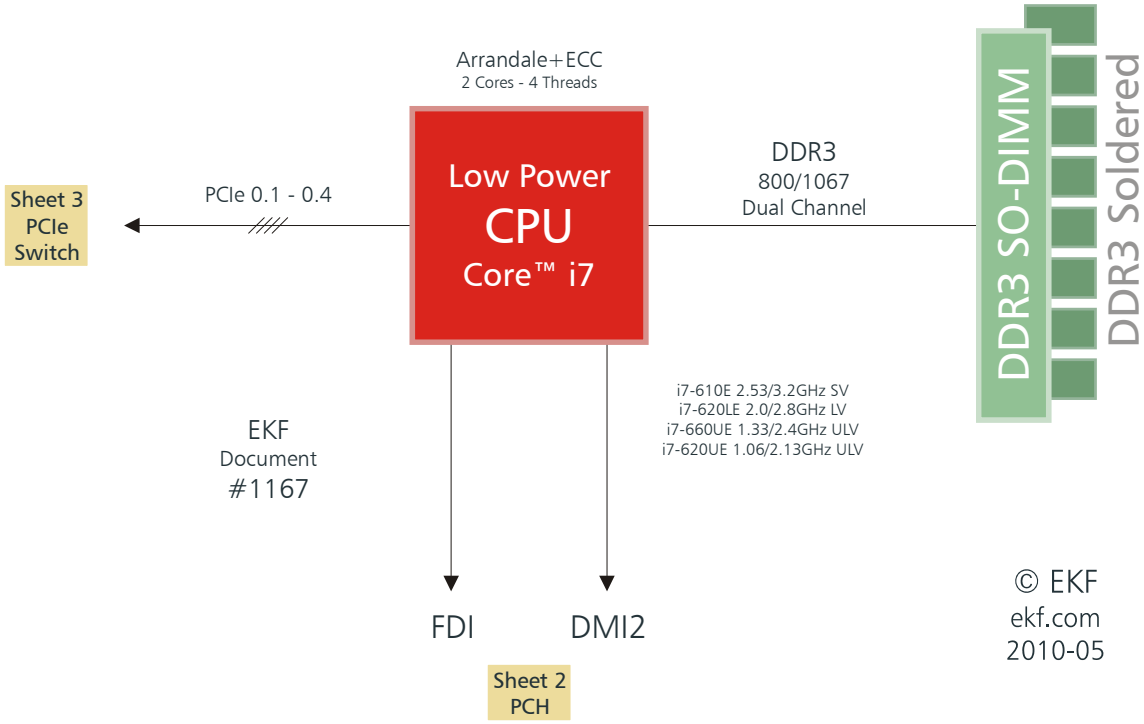
Feature Summary PC1-GROOVE	
J1 *CompactPCI*®	▸ PCH QM57 integrated 32-bit PCI bridge, 33MHz 133MBps CompactPCI master ▸ Additional PCI arbiter in PLD for fully figured 8-slot CompactPCI backplane ▸ +5V V(I/O) default configuration (PCI pull-up resistors 1k - blue coding key on J1) ▸ +3.3V V(I/O) on request (PCI pull-up resistors 2.7k - yellow coding key on J1)
CompactPCI® *Express*	▸ PC1-GROOVE can be configured as CompactPCI Express System Board (system slot controller) by optionally available mezzanine expansion card CCJ-RHYTHM ▸ CPCIe 4-Link configuration (4-lanes each), for up to 4 CPCIe peripheral slots type 1 and/or type 2 on a passive CPCIe backplane ▸ Suitable also for hybrid CPCI/CPCIe systems/backplanes (e.g. Schroff)
Platform Management	▸ Option AMT 6.0 Intel® Active Management Technology (iAMT) ▸ ARM core based Manageability Engine (ME) in the PCH QM57 ▸ Independent manageability firmware, stored in SPI Flash
Secure Computing	▸ Option Trusted Platform Module TPM 1.2 according to Trusted Computing Group specifications ▸ Available as discrete controller on several mezzanine boards e.g. CCH/CCI/CCJ ▸ Discrete crypto engine silicon brands Infineon or Atmel at users choice
Firmware	▸ Phoenix UEFI with EKF enhancements for embedded systems ▸ SPI Flash memory 2 x 16/32/64 Mb ▸ Updates available from website ekf.com
Drivers (All Major OS)	▸ Intel® graphics driver, Intel® embedded graphics driver ▸ Intel® networking driver ▸ Intel® Matrix Storage Manager software ▸ JMicron SATA driver
Drivers (All Major OS)	▸ Intel® graphics driver, Intel® embedded graphics driver ▸ Intel® networking driver ▸ Intel® Matrix Storage Manager software ▸ JMicron SATA driver
Real-Time OS BSP & Driver	▸ QNX 6.5.0 available ▸ VxWorks and others on request
Thermal Conditions Environmental Conditions	▸ Operating temperature: 0°C ... +70°C (extended temperature range on request) ▸ Storage temperature: -40°C ... +85°C, max. gradient 5°C/min ▸ Humidity 5% ... 95% RH non condensing ▸ Altitude -300m ... +3000m ▸ Shock 15g 0.33ms, 6g 6ms ▸ Vibration 1g 5-2000Hz
EC Regulations	▸ EN55022, EN55024, EN60950-1 (UL60950-1/IEC60950-1) ▸ 2002/95/EC (RoHS)

Feature Summary PC1-GROOVE					
MTBF	126 x 10^3 h (14 years) @ 50° C				
Typical Power Requirements 1) Intel® SpeedStep® Frequency Modes LFM: Low Frequency Mode, HFM: High Frequency Mode 2) Add per Ethernet port 0.2/0.6A (link only/active) @1Gbps	Board	+3.3V +0.17V/-0.1V		+5V +0.25V/-0.15V	
		MaxPower LFM/HFM 1)	Win7 Idle LFM/HFM 1)	MaxPower LFM/HFM 1)	Win7 Idle LFM/HFM 1)
	PC1-62-GROOVE	6.1/6.4A 2)	2.9/2.9A 2)	2.3/5.8A	0.1/0.1A
		S3: 250mA S4: 80mA S5: 80mA		S3: <10mA S4: <10mA S5: <10mA	
Performance Rating Measured with PCMark2005 under Windows® XP, 2 x 2GB DDR3 1066	Board	Processor		CPU/MEM Score	
	PC1-6-GROOVE	i7-610E		TBD	
	PC1-4-GROOVE	i7-620LE		TBD	
	PC1-2-GROOVE	i7-620UE		TBD	

Table items are subject to technical changes

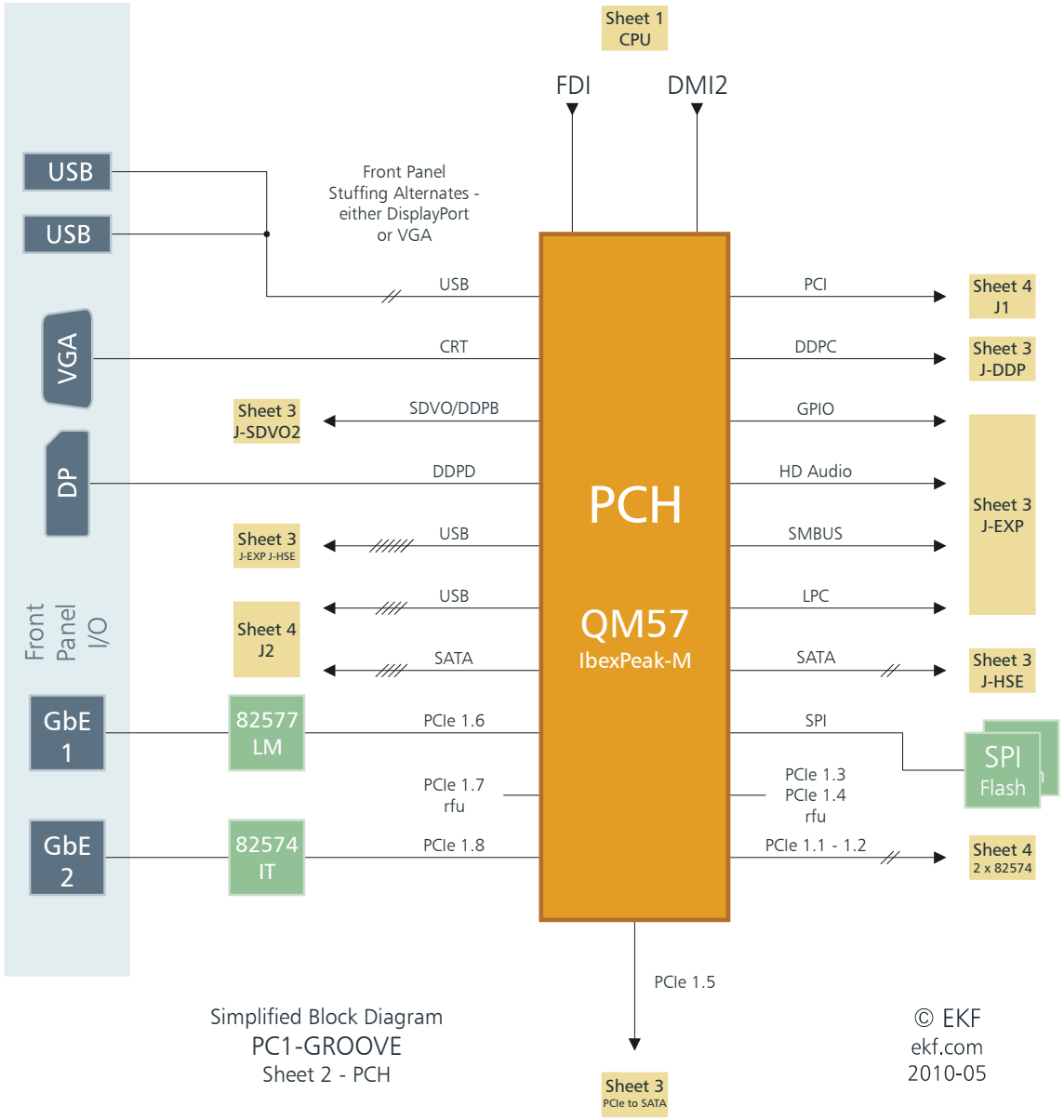
PC1-GROOVE (Option DisplayPort) and C41-CFast Module

Block Diagram PC1-GROOVE

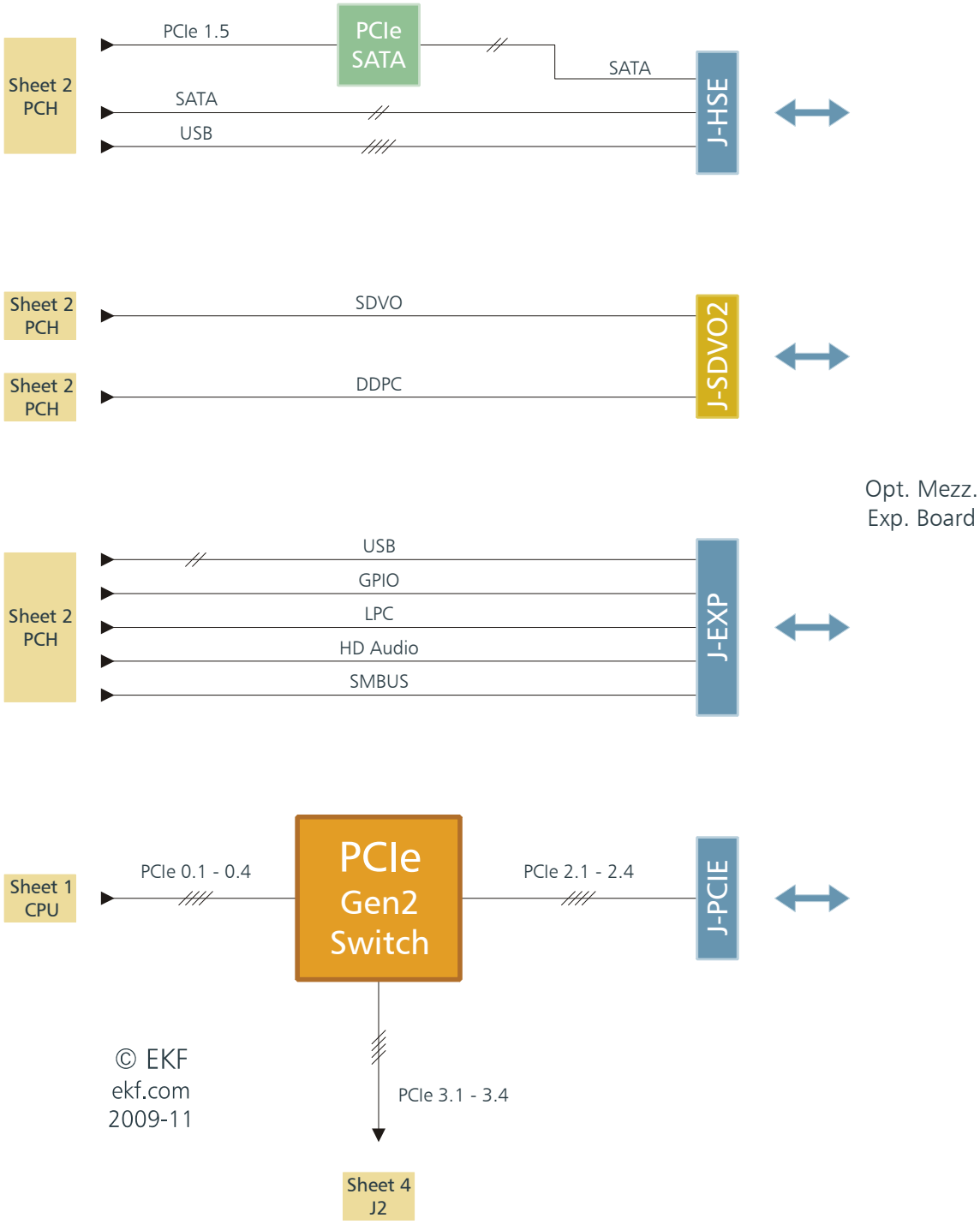


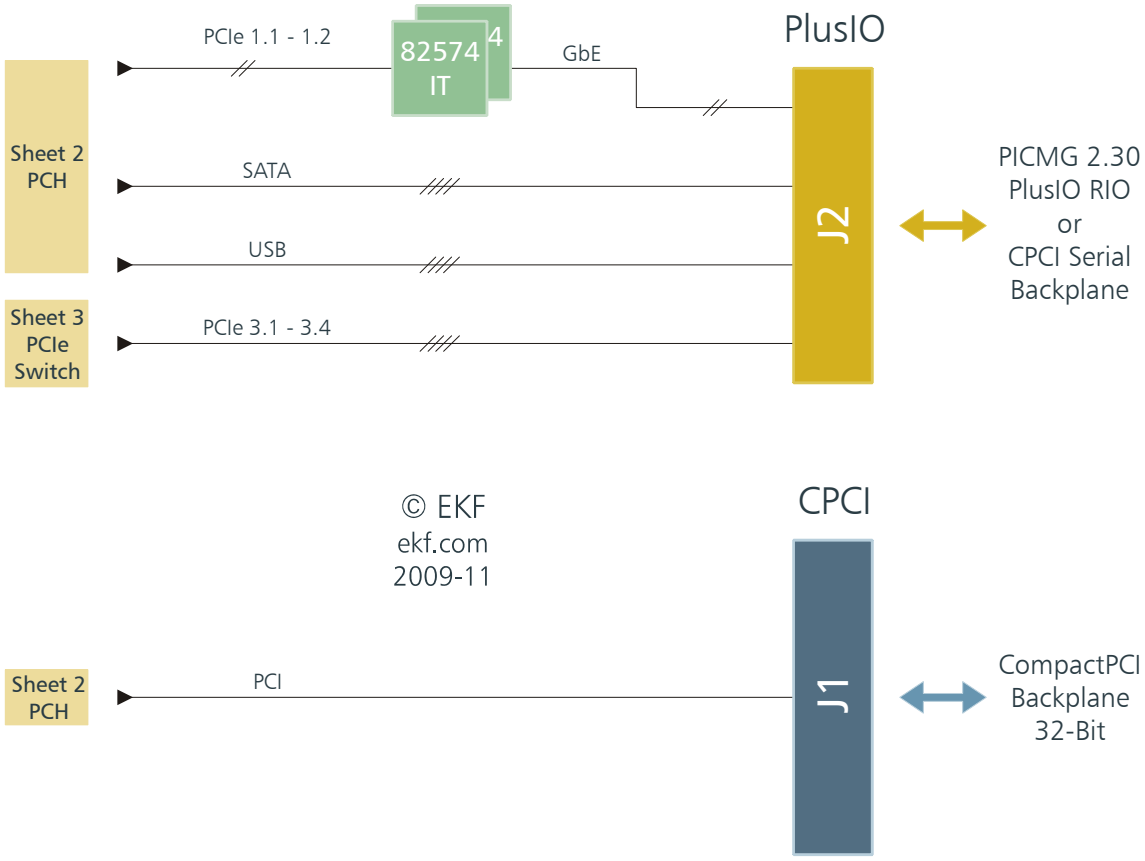
Intel® Low Power Platform Calpella+ECC

Simplified Block Diagram
PC1-GROOVE
Sheet 1 - CPU & RAM


Sheet 1
CPU
FDI
DMI2
USB
USB
Front Panel
Stuffing Alternates -
either DisplayPort
or VGA
VGA
DP
Front Panel I/O
GbE 1
GbE 2
USB
CRT
SDVO/DDPB
DDPD
USB
USB
SATA
82577 LM
82574 IT
PCIe 1.6
PCIe 1.7
rfu
PCIe 1.8
PCIe 1.5
Sheet 3
J-SDVO2
Sheet 3
J-EXP J-HSE
Sheet 4
J2
Sheet 3
PCIe to SATA
PCH
QM57
IbexPeak-M
PCI
DDPC
GPIO
HD Audio
SMBUS
LPC
SATA
SPI
PCIe 1.3
PCIe 1.4
rfu
PCIe 1.1 - 1.2
Sheet 4
J1
Sheet 3
J-DDP
Sheet 3
J-EXP
Sheet 3
J-HSE
SPI
Flash
Sheet 4
2 x 82574
Simplified Block Diagram
PC1-GROOVE
Sheet 2 - PCH
© EKF
ekf.com
2010-05

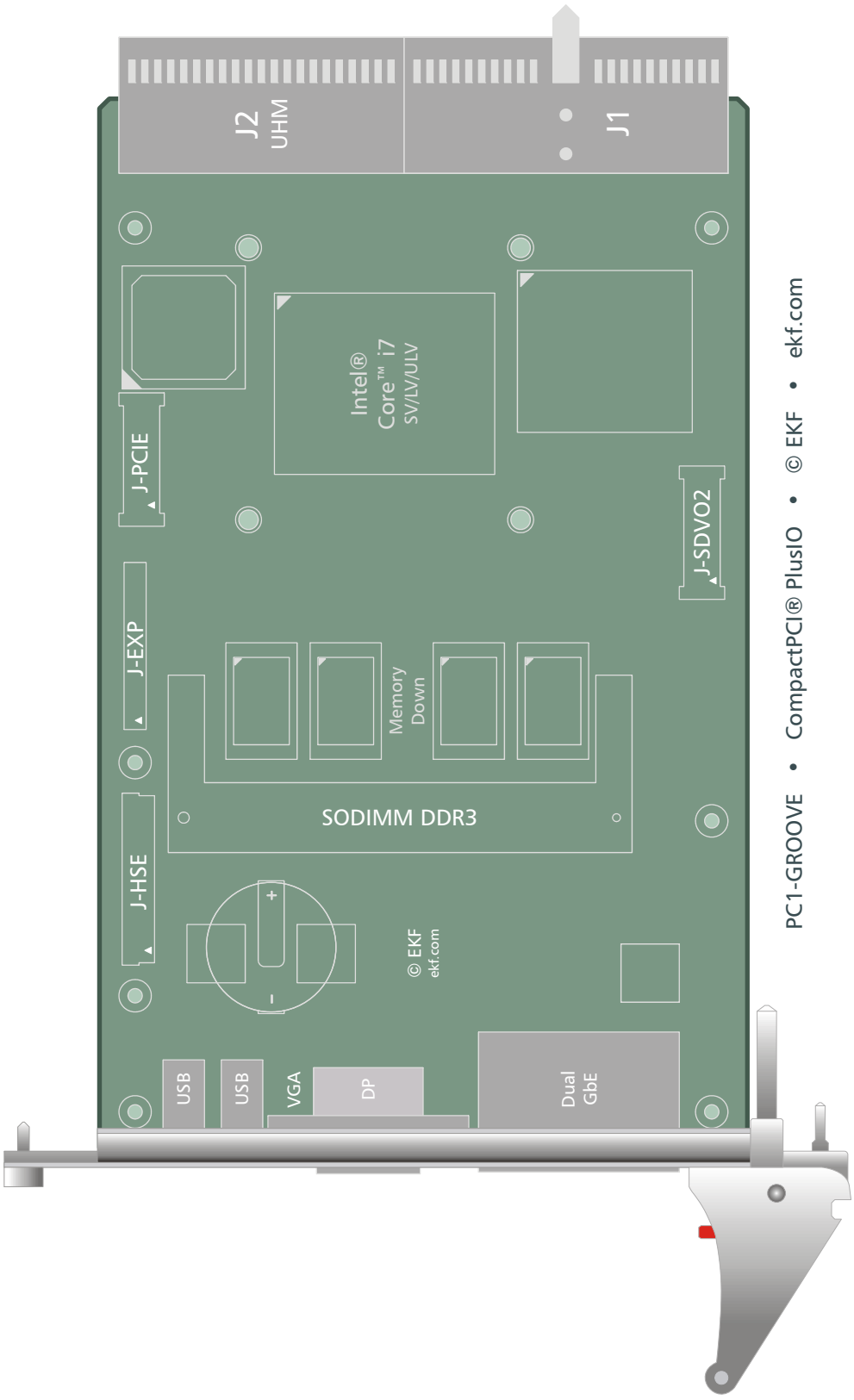
Simplified Block Diagram
PC1-GROOVE
Sheet 3 - Mezzanine Connectors



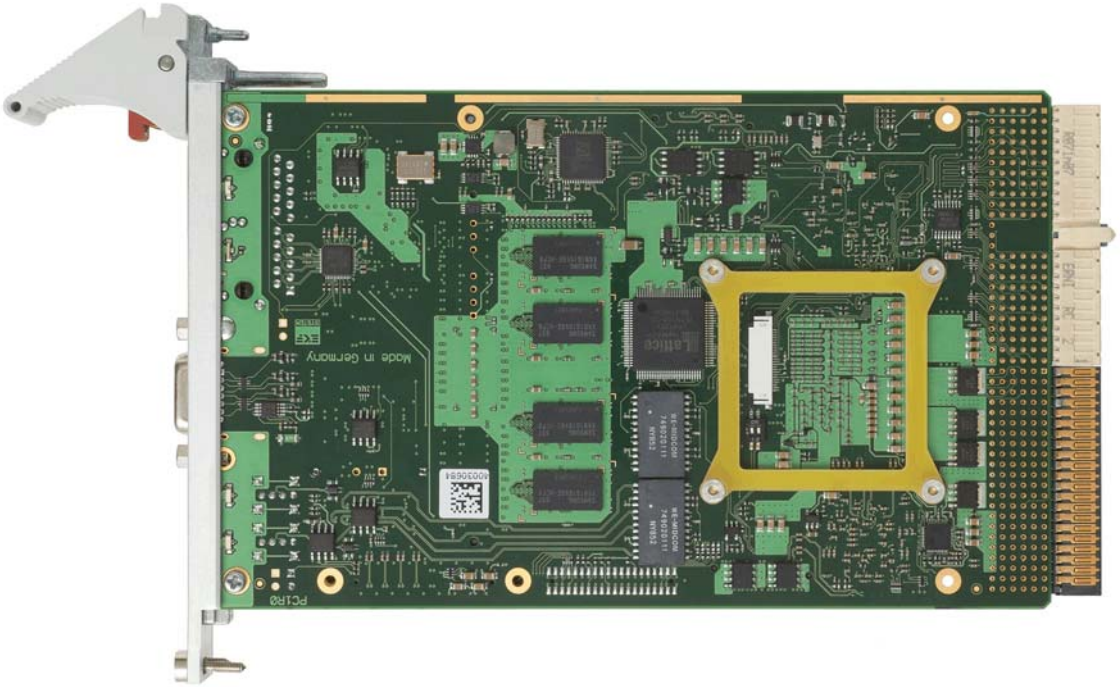


Simplified Block Diagram
PC1-GROOVE
Sheet 4 - Backplane Connectors

Top View Component Assembly



PC1-GROOVE Top View



PC1-GROOVE Bottom View

Strapping Headers

DSW1	Switches to configurate PCIe link width
P-FPH	Jumper to generate Power Button Events (Front Panel Handle Switch)
P-ISP	PLD Programming Connector, not stuffed
P-GP	Jumper to reset UEFI BIOS Setup to EKF Factory Defaults
P-MFG	Jumper to enter Manufacturing Mode, not stuffed
P-RTC	Jumper to reset RTC Core of PCH, not stuffed

Connectors & Sockets

J1/J2	*CompactPCI* Bus 32-bit, 33MHz, PlusIO
J-EXPT J-EXPB [1)]	Expansion Interface Connector (LPC Interface (Super-I/O, FWH), USB Interfaces, HD Audio Interface, SMBus), available either from top (T) or bottom (B) of the board
J-HSE	High Speed Expansion Connector (4 x SATA, 4 x USB), Interface to CompactFlash Carrier C40-SCFA and side boards
J-PCIE	PCI Express Expansion Interface Connector
J-SDVO2	Digital Display Interface Connector
SODM1	204-pin DDR3 Memory Module SDRAM PC3-8500 Socket
XDP1	CPU Debug Port

[1)] Stuffed on customers request only

Front Panel Elements

Ethernet (ETH1/2)	Dual 1000Base-TX/100Base-TX/10Base-T, RJ-45 Receptacles with integrated indicator LEDs
Graphics (DisplayPort)	DisplayPort Receptacle. Alternately available with VGA Connector.
USB1/2	Universal Serial Bus 2.0 self powered root hub, type A receptacle
EB	LED indicating PlusIO Ethernet activity
GP	General Purpose LED
HD	LED indicating any activity on SATA ports
PG	LED indicating Power Good/Board Healthy
RB	System Reset Button

Microprocessor

The PC1-GROOVE is designed for use with Intel® Core™ i7 processors (code name Arrandale). These processors integrate the graphics and memory controller within one chip that up to now were located in an external part of the chipset (GMCH). As a result the platform core is reduced from the known three chip solution (CPU, GMCH, ICH) to only two devices (CPU, PCH).

The Core™ i7 family includes beside the Standard-Voltage (SV) also several Ultra Low-Voltage (ULV) and Low-Voltage (LV) processors as listed below. The processors are housed in a Micro FC-BGA package for direct soldering to the PCB, i.e. the chip cannot be removed or changed by the user.

The processors supported by the PC1-GROOVE are running at core clock speeds up to 2.53GHz. Due to Enhanced Intel® SpeedStep® and Intel® Turbo Boost Technology each core can decrease or increase its nominal operating frequency. The internal Core™ i7 processor speed is achieved by multiplying the host base frequency of 133MHz by a variable value. The multiplier is chosen depending on the power states of the processor cores/graphics engine, the currently required performance, and the actual core temperature.

Power is applied across the *CompactPCI* connectors J1 (3.3V, 5V). The processor core voltage is generated by a switched voltage regulator, sourced from the 5V plane. The processor signals its required core voltage by 7 dedicated pins according to Intels IMVP-6.5 voltage regulator specification.

Processors Supported								
Processor	Number of Cores	Speed min/max [GHz]	L3 Cache [MB]	TDP [W]	Die Temp [°C]	CPU ID	Stepping	sSpec
ULV Core i7-620UE	2	0.67/1.06	4	18	0-105	20652h	C-2	SLBPA
ULV Core i7-660UE	2	0.67/1.33	4	18	0-105	20655h	K-0	SLBWV
LV Core i7-620LE	2	1.20/2.00	4	25	0-105	20652h	C-2	SLBP9
SV Core i7-610E	2	1.20/2.53	4	35	0-105	20652h	C-2	SLBRZ

Thermal Considerations

In order to avoid malfunctioning of the PC1-GROOVE, take care of appropriate cooling of the processor and system, e.g. by a cooling fan suitable to the maximum power consumption of the CPU chip actually in use. The processor contains digital thermal sensors (DTS) that are readable via special CPU registers. DTS allows to get the temperatures of each CPU core separately.

Two further temperature sensors located in the system hardware monitor LM87 allows for acquisition of the boards surface temperature and the thermal state of the onboard system memory channel. Beside this the LM87 also monitors most of the supply voltages. A suitable software on Microsoft Windows® systems to display both, the temperatures as well as the supply voltages, is *Speedfan*, which can be downloaded from the web. After installation, both temperatures and voltages can be observed permanently from the Windows® taskbar.

The PC1-GROOVE is equipped with a passive heatsink. Its height takes into account the 4HP limitation in mounting space of a *CompactPCI* board. In addition, a forced vertical airflow through the system enclosure (e.g. bottom mount fan unit) is strongly recommended (>20m^3/h or 2m/s (400LFM) around the CPU slot). Be sure to thoroughly discuss your actual cooling needs with EKF. Generally, the faster the CPU speed the higher its power consumption. For higher ambient temperatures, consider increasing the forced airflow to 3m/s (600LFM) or more.

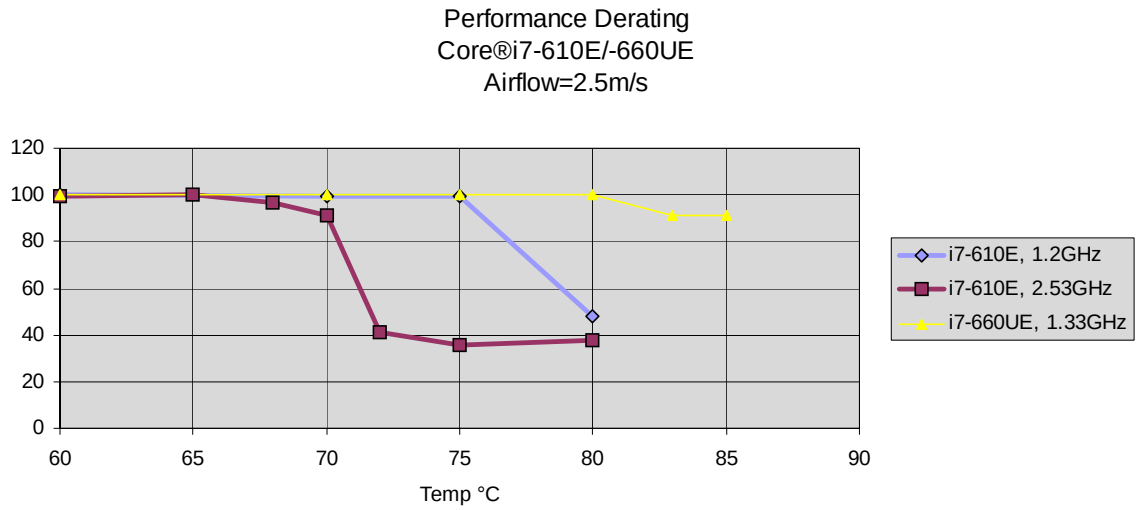
The table showing the supported processors above give also the maximum power consumption (TDP = Thermal Design Power) of a particular processor. Fortunately, the power consumption is by far lower when executing typical Windows® or Linux tasks. The heat dissipation increases when e.g. rendering software like the Acrobat Distiller is executed.

The Core™ i7 processors support Intel's Enhanced SpeedStep® technology. This enables dynamic switching between multiple core voltages and frequencies depending on core temperature and currently required performance. The processors are able to reduce their core speed and core voltage in multiple steps down to 1200MHz (667MHz for ULV processors). This leads to an obvious reduction of power consumption resulting in less heating. This mode of lowering the processor core temperature is called TM2 (TM=Thermal Monitor).

Another way to reduce power consumption is to modulate the processor clock. This mode (TM1) is achieved by actuating the 'Stop Clock' input of the CPU. A throttling of 50% e.g. means a duty cycle of 50% on the stop clock input. However, while saving considerable power consumption, the data throughput of the processor is also reduced. The processor works at full speed until the core temperature reaches a critical value. Then the processor is throttled by 50%. As soon as the high temperature situation disappears the throttling will be disabled and the processors runs at full speed again.

These features are controllable by BIOS menu entries. By default the BIOS of the PC1-GROOVE enables mode TM2 which is the most efficient.

The following diagram shows the performance derating with increasing temperature for an i7-610E processor running at its maximum (2.53GHz) and minimum (1.20GHz) frequency as well as an i7-660UE ULV processor at 1.33GHz.



Main Memory

The PC1-GROOVE features two channels of DDR3 SDRAMs. One channel is realized with 8 memory devices soldered to the board (Memory Down) and delivers a capacity of up to 4GB with a clock frequency of 1066MHz (PC3-8500).

The 2nd channel provides a socket for installing a 204-pin SODIMM module thus allowing a simple expansion of system memory (max. module height = 1.25 inch). Supported are unbuffered DDR3 SODIMMs (V_{CC}=1.5V) without ECC featuring on-die termination (ODT), according the PC3-6400 or PC3-8500 specification. Minimum module size is 512MB; maximum module size is 4GB.

It is recommended to add a SODIMM module with same size as the Memory Down to get best performance (some of the system memory is dedicated to the graphics controller). This typically results in a size of 2x1GB of memory which is recommended to run the operating systems Windows® XP, Windows® Vista or Windows® 7.

The memory controller supports symmetric and asymmetric memory organization. The maximum memory performance can be obtained by using the symmetric mode. When in this mode, the memory controller accesses the memory channels in an interleaved way. Since Core™ i7 processors support Intels Flex Memory Technology, interleaved operation isn't limited to systems using memory channels of equal capacity. In the case of unequal memory population the smaller memory channel dictates the address space of the interleaved accessible memory region. The remainder of the memory is then accessed in non-interleaved mode.

In asymmetric mode the memory always will be accessed in a non-interleaved manner with the drawback of less bandwidth. The only meaningful application of asymmetric mode is the special case when only one memory channel is populated (i.e. the SODIMM socket may be left empty).

The contents of the SPD EEPROM on the SO-DIMM is used by the BIOS at POST (Power-on Self Test) to get any necessary timing parameters to program the memory controller within the chipset.

Graphics Subsystem

The graphics subsystem is part of the Intel Core™ i7 processor and the PCH QM57. While the graphics controller is located within the Core™ i7 processor, the different interfaces like DisplayPort, SDVO and VGA are moved to the PCH. The PC1-GROOVE offers one DisplayPort interface in the front panel.

Adapters to convert DisplayPort to any other popular interface standard are available.

A 2nd DisplayPort and an SDVO port is fed to the on-board connector J-SDVO2. Currently expansion boards like CCH-MARIACHI feature the display transmitter to provide a DVI channel via a pure digital DVI-D connector. Future EKF expansion boards will feature also the possibility to gain access to a 2nd DisplayPort interface.

As an option, the PC1-GROOVE can be equipped with an ordinary HD D-Sub 15-lead connector (VGA style). This connector is suitable for analog signals only. Nevertheless also flat-panel displays can be attached to the D-Sub connector but with minor reduced image quality.

Independent from the video connector actually in use, DisplayPort, DVI or VGA, the VESA DDC standard is supported. This allows to read out important parameters, e.g. the maximum allowable resolution, from the attached monitor. If stuffed, DDC Power (+5V) is delivered to the legacy VGA connector. A resettable fuse is used to protect the board from an external short-circuit condition (0.5A).

Graphics drivers for the Core™ i7 can be downloaded from the Intel web site.

LAN Subsystem

The Ethernet LAN subsystem is composed of four Gigabit Ethernet ports: One Intel 82577LM Physical Layer Transceiver (PHY) using the PCH QM57 internal MAC and three Intel 82574L Gigabit Ethernet Controllers. These devices provide also legacy 10Base-T and 100Base-TX connectivity. Two of the Ethernet ports are fed to two RJ45 jacks located in the front panel, the others are attached to the PlusIO interface on J2/P2. Each port includes the following features:

- One PCI Express lane per Ethernet port (250MB/s)
- 1000Base-Tx (Gigabit Ethernet), 100Base-TX (Fast Ethernet) and 10Base-T (Classic Ethernet) capability.
- Half- or full-duplex operation.
- IEEE 802.3u, 802.3ab Auto-Negotiation for the fastest available connection.
- Jumperless configuration (complete software-configurable).

Two bicoloured LEDs integrated into the dedicated RJ-45 connector in the front panel are used to signal the LAN link, the LAN connection speed and activity status. A further bicoloured LED in front panel labelled EB displays the state of the PlusIO network ports.

Each device is connected by a single PCI Express lane to the PCH. Their MAC addresses (unique hardware number) are stored in dedicated FLASH/EEPROM components. The Intel Ethernet software and drivers for the 82577 and 82574 is available from Intel's World Wide Web site for download.

When managing the board by Intel Active Management Technology (iAMT), the dedicated network port to do so is accessible by the RJ45 connector GbE1 (the upper port within the front panel).

Serial ATA Interface (SATA)

The PC1-GROOVE provides eight serial ATA (SATA) ports each capable of transferring 3Gbps (300MByte/s). Four of the six ports integrated within the PCH are routed to the *CompactPCI* PlusIO interface (J2/P2 connector). The remainder SATA channels of the PCH and two further ports coming from an additional controller (JMicron JMB362) are fed to the high speed expansion connector J-HSE. This connector allows the installation of local expansion boards like C40-SCFA to attach the popular CompactFlash cards.

A LED named HD located in the front panel, signals disk activity status of the SATA devices.

Available for download from Intel's and JMicron's web sites are drivers for popular operating systems, e.g. Windows® XP, Windows® Vista, Windows® 7 and Linux.

PCI Express Interface (PCIe)

On PC1-GROOVE four PCI Express lanes, originating from the Core™ i7 processor, are building one upstream link to a PCI Express switch. The output ports (downstream ports) of the PCIe switch are connected to the *CompactPCI* PlusIO connector J2/P2 (four lanes) and to the local PCIe expansion interface connector J-PCIE (four lanes).

Two small DIP switches (DSW1) located on the backside of the board are used to configure different lane widths to each of both downstream interfaces. Possible settings are

- A single link x 4 lanes to J2/P2 and a single link x 4 lanes to J-PCIE
- Four links x 1 lane to J2/P2 and a single link x 4 lanes to J-PCIE
- Four links x 1 lane to J2/P2 and four links x 1 lane to J-PCIE

See section "*Configuration Switches PCI Express Link Width (DSW1)*" for details.

While the link speed on the upstream side of the switch is restricted to 2.5GT/s due to limitations of the PCH QM57, the downstream ports may support also PCIe Gen 2 speed (5GT/s).

Universal Serial Bus (USB)

The PC1-GROOVE is provided with twelve USB ports, all of them are USB 2.0 capable. Two USB interfaces are routed to front panel connectors, two ports are feed to the expansion board interface connectors J-EXP, four to the high speed expansion connector J-HSE, and four ports are available across the J2/P2 connector for PlusIO.

The front panel USB connectors can source up to 0.5A/5V each, over-current protected by two electronic switches. Protection for the USB ports on the expansion interfaces and on the PlusIO connector is located on expansion boards like CCH-MARIACHI and the boards on the *CompactPCI* Serial backplane respective. The two USB EHCI controllers handling the USB ports are integrated into the PCH.

Real-Time Clock

The PC1-GROOVE has a time-of-day clock and 100-year calendar, integrated into the PCH. A battery on the board keeps the clock current when the computer is turned off. The PC1 uses a BR2032 lithium battery soldered in the board, giving an autonomy of more than 5 years. Under normal conditions, replacement should be superfluous during lifetime of the board.

In applications were the use of a battery is not permitted, a SuperCap can be stuffed instead of the battery.

LPC Super-I/O Interface

In a modern system, legacy ports like PS/2 keyboard/mouse, COM1/2 and LPT have been replaced by USB and Ethernet connectivity. Hence, the PC1-GROOVE is virtually provided with all necessary I/O ports. However, for compatibility purposes the PC1 is equipped with the interface connector J-EXP to the local LPC bus (LPC = Low Pin Count interface standard), which is a serialized ISA bus replacement.

EKF offers multiple expansion boards to the PC1-GROOVE, featuring all classic Super-I/O functionality, for example the CCH-MARIACHI. Access to the connectors PS/2 (mouse, keyboard), COM, USB and audio in/out is given directly from the front panel. The CCH-MARIACHI connects to the PC1-GROOVE across the connectors P-EXPT or P-EXPB. Usually the CCH is attached to the top of the PC1-GROOVE. Nevertheless bottom side mounting is possible on customers request.

SPI Flash

The BIOS is stored in two flash devices with Serial Peripheral Interface (SPI). 8MByte of BIOS code, AMT firmware and user data may be stored nonvolatile in these SPI flashs (up to 16MByte of flash space is available on request).

The SPI flash contents can be reprogrammed (if suitable) by a DOS or Linux based tool. This program and the latest PC1-GROOVE BIOS binary are available from the EKF website. Read carefully the enclosed instructions. If the programming procedure fails e.g. caused by a power interruption, the PC1-GROOVE may no more be operable. In this case you would possibly have to send in the board, because the flash devices are directly soldered to the PCB and cannot be changed by the user.

Reset

The PC1-GROOVE is provided with several supervisor circuits to monitor supply rails like the CPU core voltage, 1.5V, 3.3V or 5V. This circuitry is responsible also to generate a clean power-on reset signal.

To force a manual board reset the PC1-GROOVE offers a small tactile switch within the front panel. This push-button is indent mounted and requires a tool, e.g. a pen to be pressed, preventing from being inadvertently activated.

The ejector within the front panel contains a micro switch that is used to generate a power button event. This is done by pushing the red button of the ejector until the handle unlocks without ejecting the board. Immediately after that push up the ejector back to its original position (the red button jumps up as well). Animated GIF: www.ekf.com/c/ccpu/img/reset_400.gif

NOTE: To prevent the board to cause a power button override, the handle should be closed immediately after unlocking the front panel handle. A power button override is triggered by opening the front panel handle for at least 4 seconds. It results in bringing the board to power state S5. In case of entering this state, unlock and lock the front panel handle a 2nd time to reenter normal power state S0 again. See also section 'PG (Power Good) LED' to see how the PC1-GROOVE indicates the different power states.

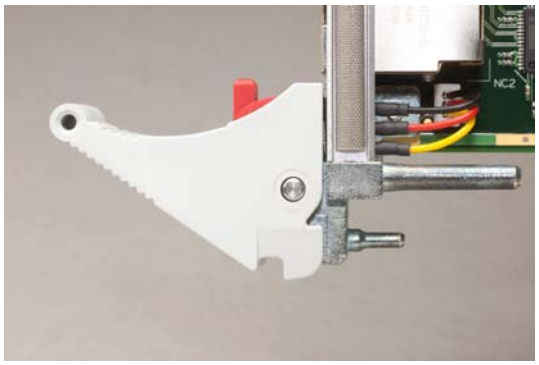
WARNING: The PC1-GROOVE will enter the power state S5 if the front panel handle is not closed properly when the system powers up. An open handle is signalled by a yellow blinking ‘PG LED’.

The manual reset push-button and the power button functionality of the front panel handle could be passivated by BIOS settings.

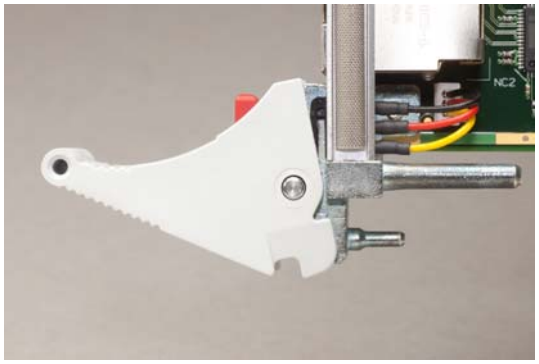
An alternative (and recommended) way to generate a system reset is to activate the signal PRST# located on *CompactPCI* connector J2 pin C17. Pulling this signal to GND will have the same effect as to push the tactile reset switch.

The healthy state of the PC1-GROOVE is indicated by the LED PG (Power Good) located in the front panel. This bicoloured LED signals different states of the board (see section below). As soon as this LED begins to shine green all power voltages are within their specifications and the reset signal has been deasserted.

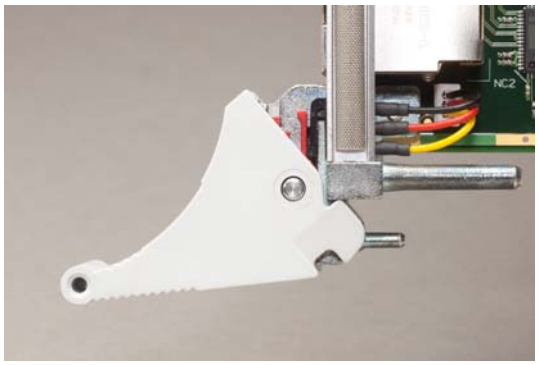

ETH
PC1
GROOVE

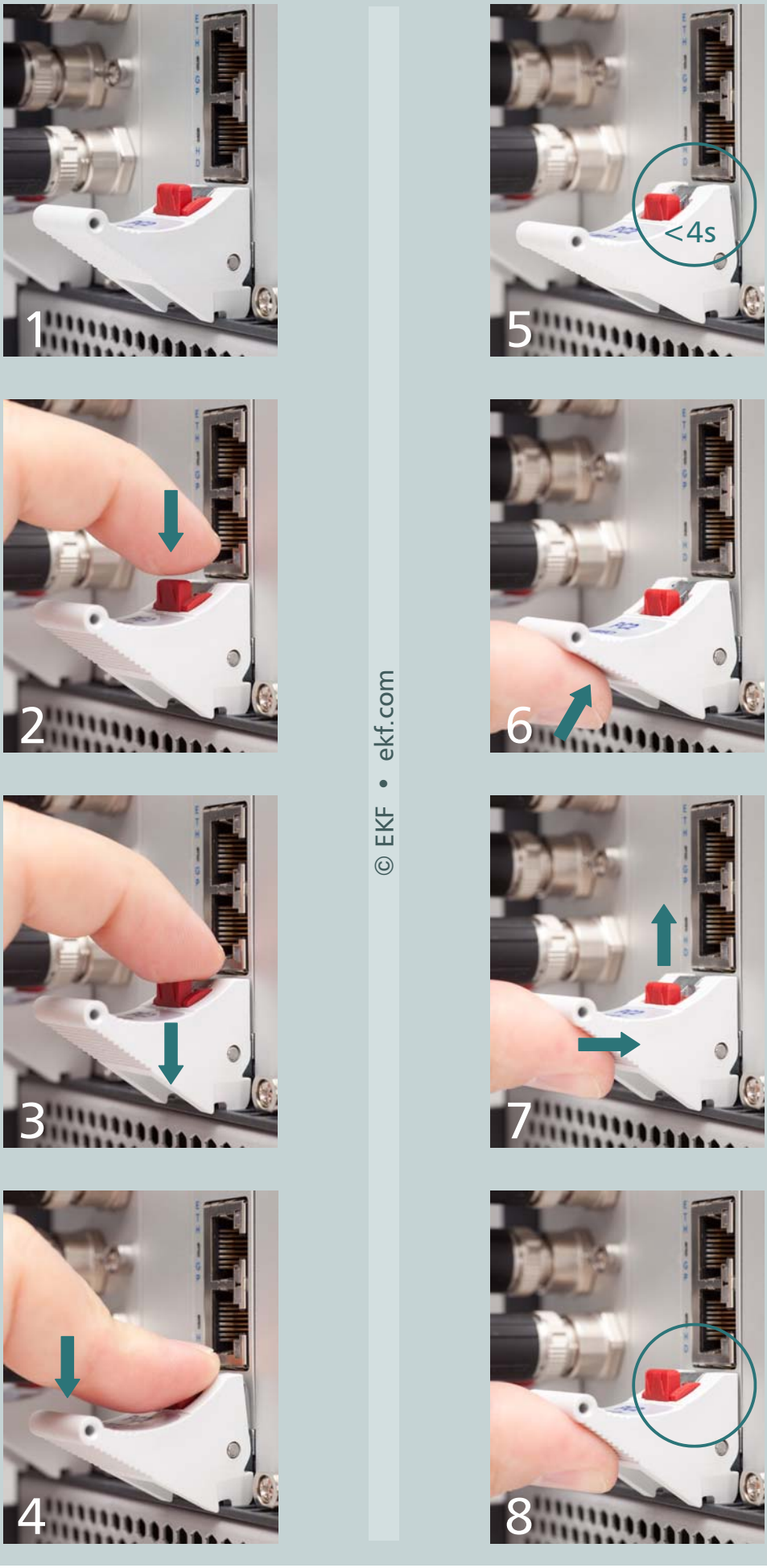

NC2


ETH
PC1
GROOVE


NC2


ETH
PC1
GROOVE


NC2


1
2
3
4
<4s
5
6
7
8
© EKF • ekf.com

Watchdog

An important reliability feature is the watchdog function, which is programmable by software. The behaviour of the watchdog is defined within the PLD, which activates/deactivates the watchdog and controls its time-out period. The time-out delay is adjustable in the steps 2, 10, 50 and 255 seconds. After alerting the WD and programming the time-out value, the related software (e.g. application program) must trigger the watchdog periodically. To simplify watchdog programming all watchdog related functions can be done by calling service requests (software SMI's).

The watchdog is in a passive state after a system reset. There is no need to trigger it at boot time. The watchdog is activated on the first trigger request. If the duration between two trigger requests exceeds the programmed period, the watchdog times out and a full system reset will be generated. The watchdog remains in the active state until the next system reset. There is no way to disable it once it has been put on alert, whereas it is possible to reprogram its time-out value at any time.

PG (Power Good) LED

The PC1-GROOVE offers a LED labelled PG located within the front panel. After system reset, this LED defaults to signal different power states:

- Off Sleep state S3, S4 or S5
- Red steady Hardware failure
- Red blink Software failure
- Yellow blink Front panel handle is unlocked
- Green Healthy

In the state *Off* the LEDs GP and HD decode the kind of sleep state as follows:

State	Description	LED GP	LED HD
S3	Suspend to RAM/Standby	OFF	ON
S4	Suspend to Disk/Hibernate	ON	OFF
S5	Soft Off	ON	ON

To enter the PG LED state *Software failure* an appropriate service request by software SMI must be called. The PG LED remains in this red blinking state until the next SMI request is made. After that it falls back to its default function.

HD (Hard Disk Activity) LED

The PC1-GROOVE offers a LED marked as HD placed within the front panel. This LED signals activity on any device attached to the SATA ports. Since the HD activity display is realized as a bicolour LED the access of devices connected to PCH QM57 or the SATA-Controller JMB362 can be distinguished in the following way:

- Off no activity
- Green access to PCH SATA Ports
- Yellow access to JMB362 SATA Ports

As described above this LED may change its function dependent on the state of the LED PG.

GP (General Purpose) LED

Another programmable bicoloured LED can be observed from the front panel. The status of the red part within the GP LED is controlled by the GPO18 output of the PCH. Setting this pin to "1" will switch on the red LED. To turn on or off the green LED an appropriate service request (software SMI) must be made.

While the CPU card is controlled by the BIOS firmware, the GP LED is used to signal board status information. A red blinking GP LED is an indication that the BIOS code couldn't start. For details please refer to www.ekf.com/p/pc1/firmware/biosinfo.txt. After successful operating system boot, the GP LED is not dedicated to any particular hardware or firmware function with exception of special states of the LED PG as described above. Hence it may be freely used by customer software.

EB (Ethernet Backplane) LED

To monitor the link status and activity on both Ethernet ports attached to the backplane via the J2/P2 connector (PlusIO) a single bicoloured LED is provided in the front panel. The states are decoded as follows:

1_ETH	2_ETH	LED EB
no link	no link	OFF
link	no link	Green
no link	link	Yellow
link	link	Green/Yellow

Blinking of the LED EB in the appropriate colour means that there is activity on the port.

Hot Swap Detection

The *CompactPCI* specification added the signal ENUM# to the PCI bus to allow board hot swapping. This signal is routed to the GPI3 of the PCH. A System Management Interrupt (SMI) can be requested if ENUM# changes by insertion or removal of a board.

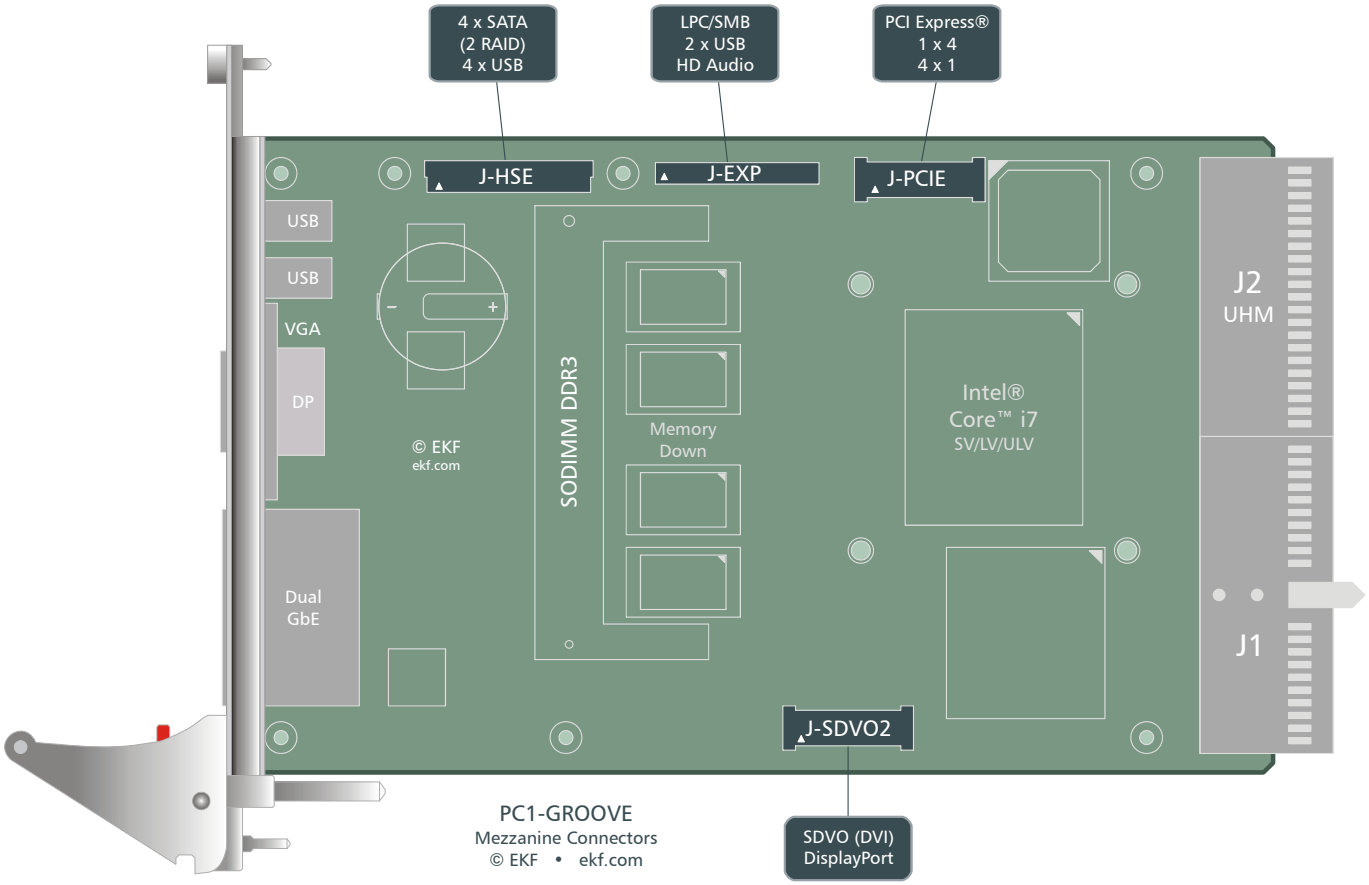
Note that the PC1-GROOVE itself is not a hot swap device, because it makes no sense to remove the system controller from a *CompactPCI* system. However, it is capable to recognize the hot swap of peripheral boards and to start software that is doing any necessary system reconfiguration.

Power Supply Status (DEG#, FAL#)

Power supply failures may be detected before the system crashes down by monitoring the signals DEG# or FAL#. These active low lines are additions of the *CompactPCI* specification and may be driven by the power supply. DEG# signals the degrading of the supply voltages, FAL# their possible failure. On the PC1-GROOVE the signals FAL# and DEG# are routed to the PCH GPI4 and GPI5 respectively.

Mezzanine Side Board Options

The PC1-GROOVE is provided with several stacking connectors for attachment of a mezzanine expansion module (aka side board), suitable for a variety of readily available mezzanine cards (please refer to www.ekf.com/c/ccpu/mezz_ovw.pdf for a more comprehensive overview). EKF furthermore offers custom specific development of side boads (please contact sales@ekf.de).

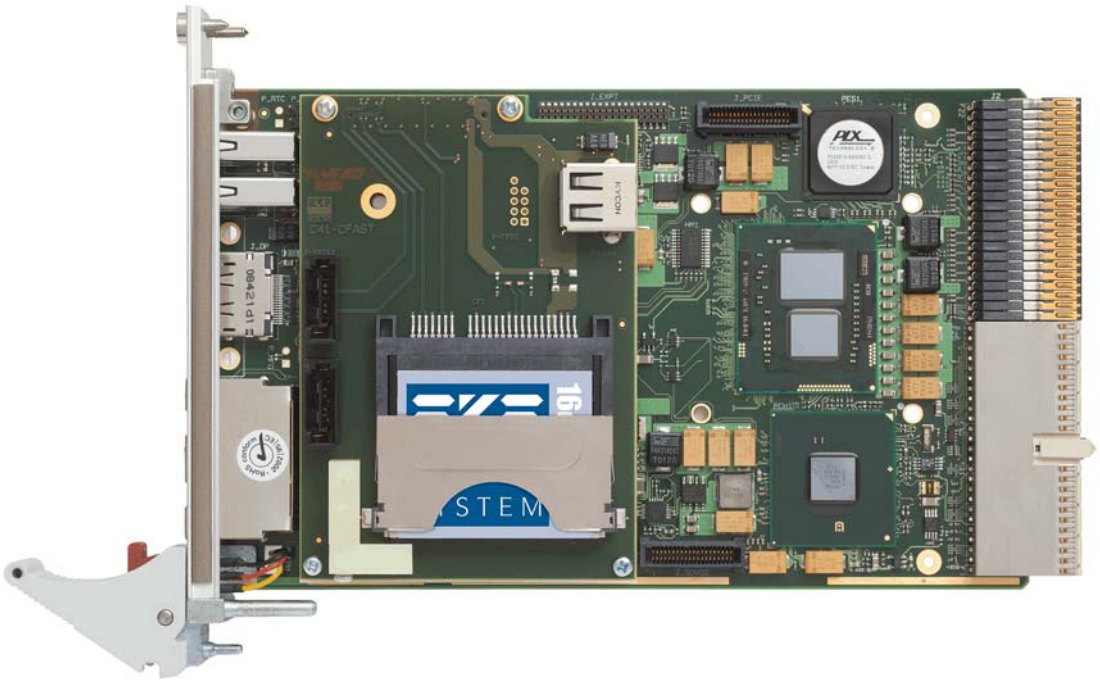


Most mezzanine expansion modules require an assembly height of 8HP in total, together with the CPU carrier board (resulting from two cards at 4HP pitch each).

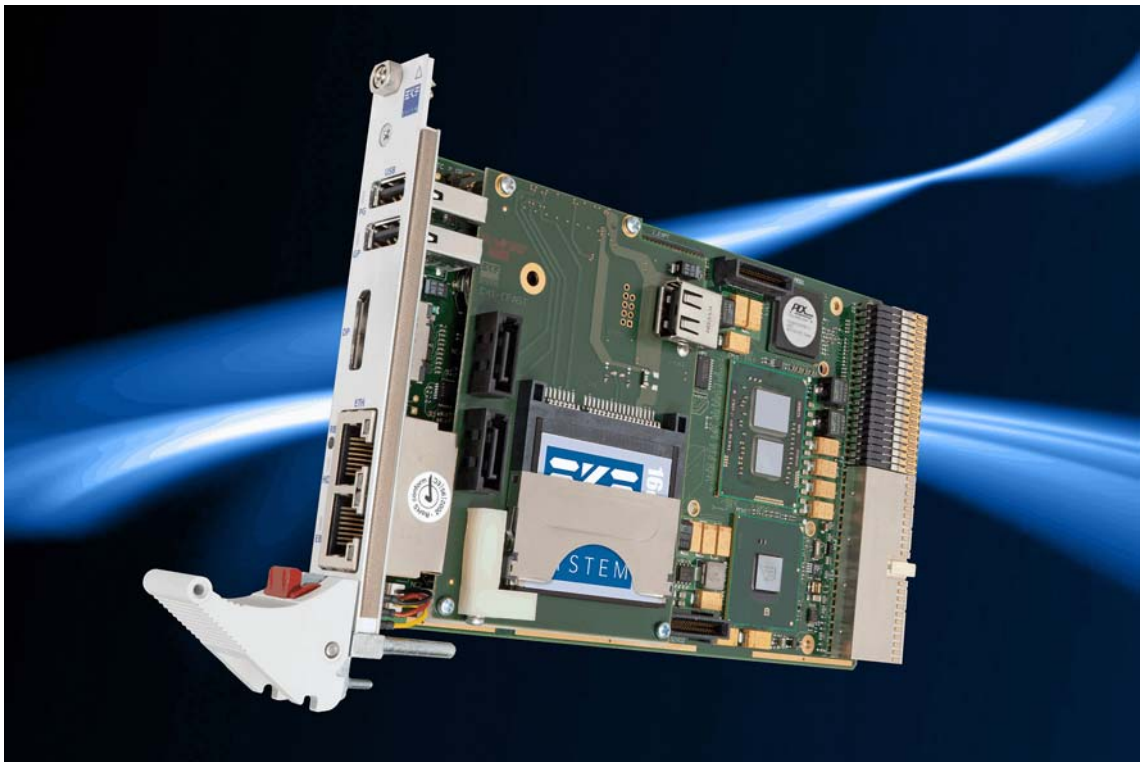
In addition, cropped mezzanine modules are available for mass storage, which maintain the 4HP envelope (see illustrations next page), for extremely compact systems. Furthermore these small size modules may be combined with the full-size expansion boards (that means an assembly comprised of 3 PCBs).

Low Profile Storage Module Area

PC1-GROOVE with C47-MSATA RAID Mezzanine Module



PC1-GROOVE w. C41-CFAST Mezzanine Module



PC1-GROOVE w. C41-CFAST Mezzanine Module

PC1-GROOVE w. C42-SATA Mezzanine Module

Related Documents Mezzanine Modules and Side Cards	
C40 ... C45 Series Mezzanine Storage Modules	www.ekf.com/c/ccpu/c4x_mezz_ovw.pdf
Mezzanine Modules Overview	www.ekf.com/c/ccpu/mezz_ovw.pdf

C41-CFAST Mezzanine Module

C42-SATA Mezzanine Module

C43-SATA Mezzanine Module

PC1-GROOVE • C44-SATA Side Card

C45-SATA Side Card

PC1-GROOVE • C45-SATA (Removable SSD)

PC1-GROOVE • C45-SATA (Internal SSD)

Custom Specific Mezzanine Module Design

CompactPCI® PlusIO Option

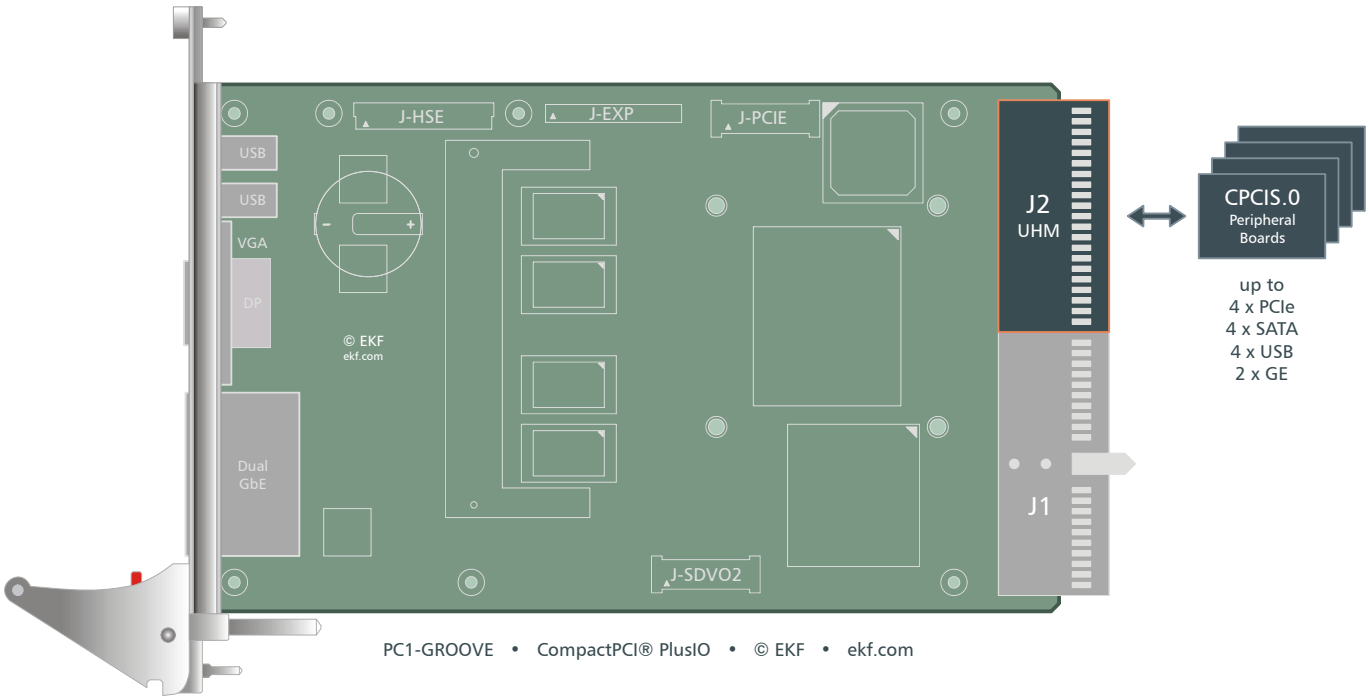
The PICMG® 2.30 CompactPCI® PlusIO specification defines the usage of rear I/O pins of the 32-bit CompactPCI® system slot for high-speed serial signals. For these high-speed signals a new J2 connector (3M UHM type) has been introduced, which is compatible to the classic 2.0mm hard metric connector J2, and in addition is suitable for high speed differential signals.

The main advantage of the combination of legacy PCI (J1/P1) and modern serial buses on J2/P2 is to realize hybrid backplanes. Hence, the CompactPCI® PlusIO standard helps to define a simple migration path from parallel PCI systems to modern serial, point-to-point interconnected systems such as CompactPCI® Serial (PICMG® CPCI-S.0, draft/proposal as of current).

PICMG® 2.30 defines just the system slot J2/P2 extension. With respect to high speed signal peripheral boards – depending on their particular interfaces – CompactPCI® Serial, CompactPCI® Express or PICMG® 2.16 cards may be combined in a system, in addition to 32-bit classic CompactPCI® boards, controlled across J1/P1.

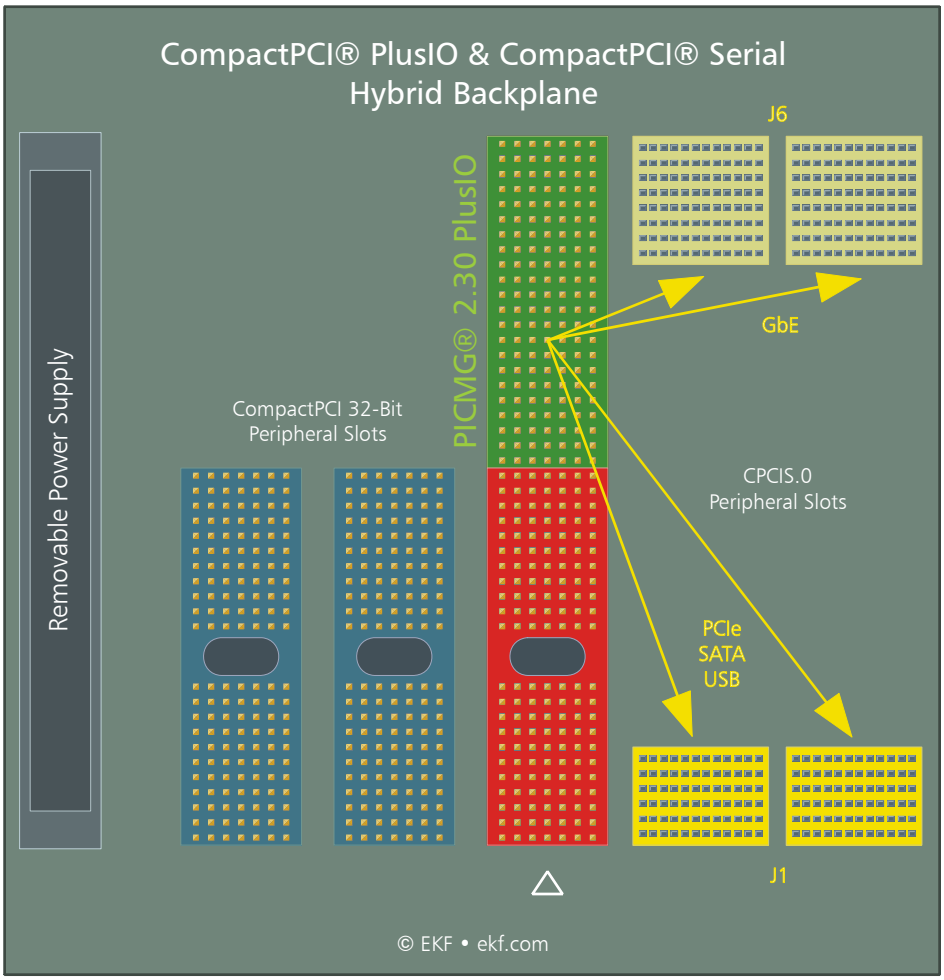
The PC1-GROVE is provided with all CompactPCI® PlusIO communication channels defined by PICMG® 2.30 via the connector J2/P2:

- Four PCIe Lanes 2.5GT/s or 5GT/s
- Four SATA Ports 3GT/s
- Four USB 2.0 Ports
- Two Gigabit Ethernet Ports



Warning: Do not operate the PC1-GROOVE in systems with a 64-bit CompactPCI® backplane. The J2/P2 pin assignments of a 64-bit CPCI backplane differ substantially from a CompactPCI® PlusIO backplane, which may result in a short circuit situation.

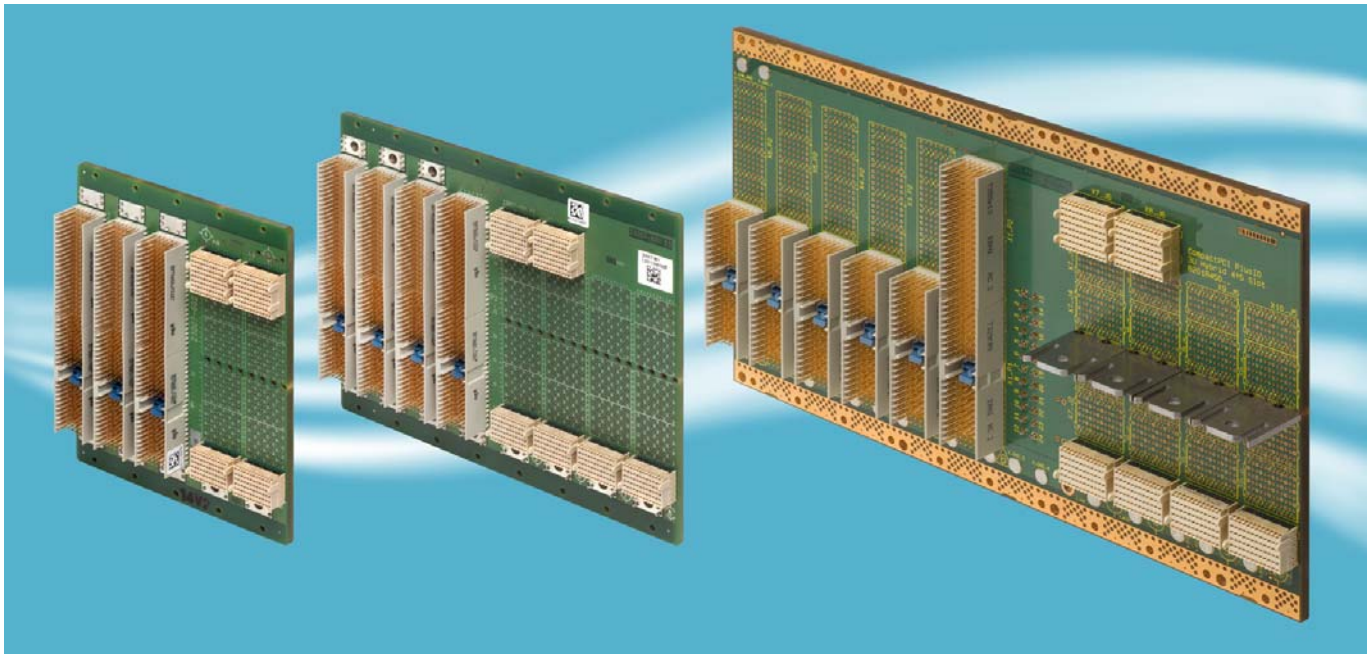
The PC1-GROOVE can be used in any system with a CompactPCI® PlusIO backplane according to the PICMG® 2.30 specification. Hybrid backplanes allow the configuration of systems with CompactPCI® Serial slots in addition to classic CompactPCI® boards.



Sample Small Systems Hybrid Backplane

Related Documents CompactPCI® PlusIO & CompactPCI® Serial	
CompactPCI® Serial - Concise Guide	www.ekf.com/s/serial_concise.pdf
CompactPCI® Serial - The Smart Solution	www.ekf.com/s/smart_solution.pdf
CompactPCI® Serial Home	www.ekf.com/s/serial.html
CompactPCI® PlusIO Home	www.ekf.com/p/plus.html

PC1-GROOVE as System Controller in a Hybrid System



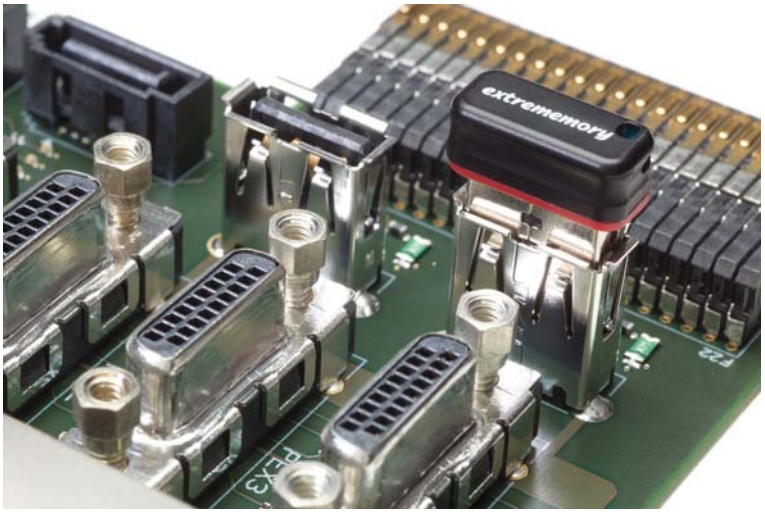
Sample Hybrid CompactPCI® & CompactPCI® Serial Backplanes

Sample Hybrid System Rack

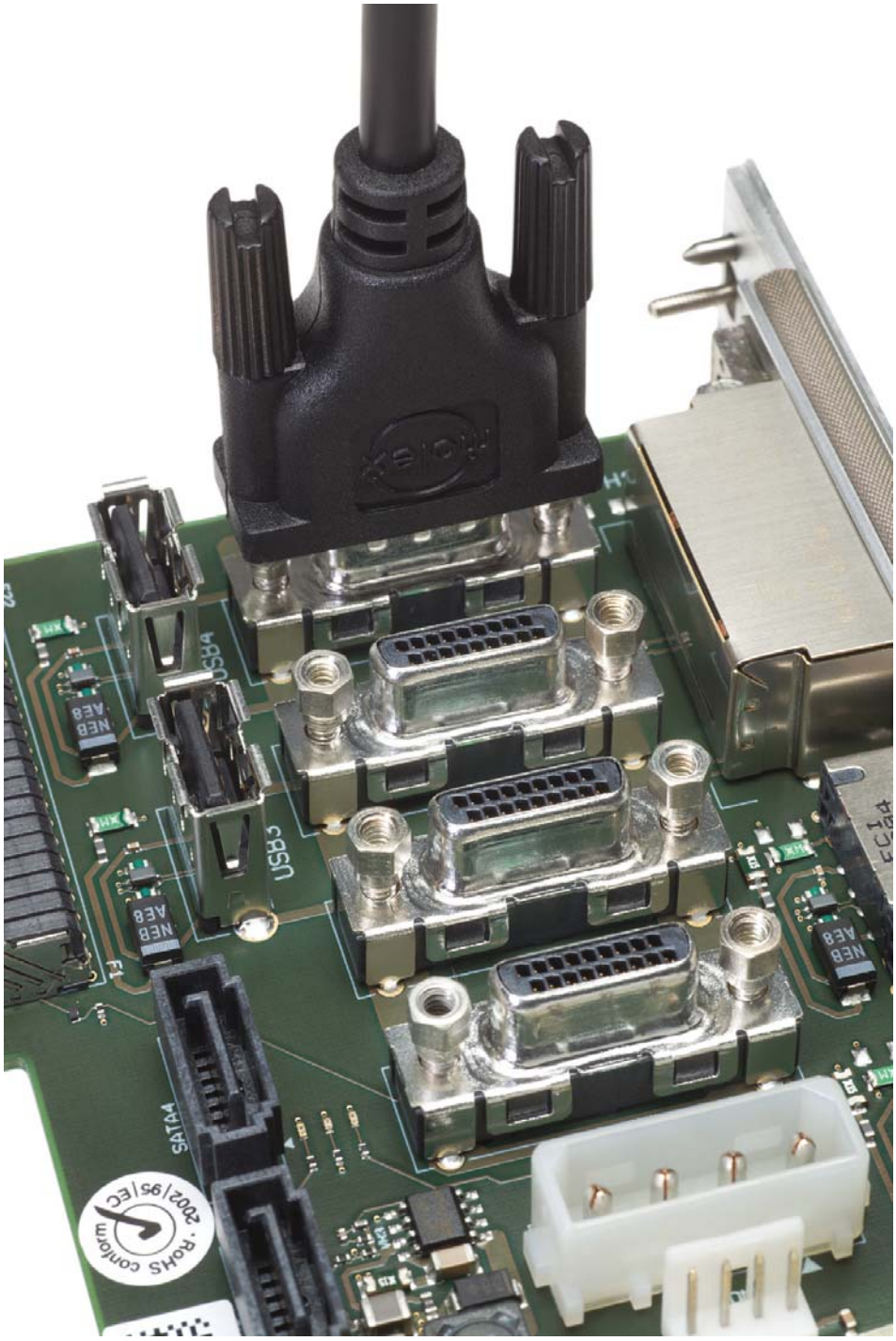
Sample Hybrid System Rack

As an alternate, the PC1-GROOVE can be combined with a CompactPCI® PlusIO rear I/O transition module, such as the PR1-RIO, which is provided with I/O connectors (on-board and back-panel) for all high speed signals.

PR1-RIO • Rear I/O Transition Module

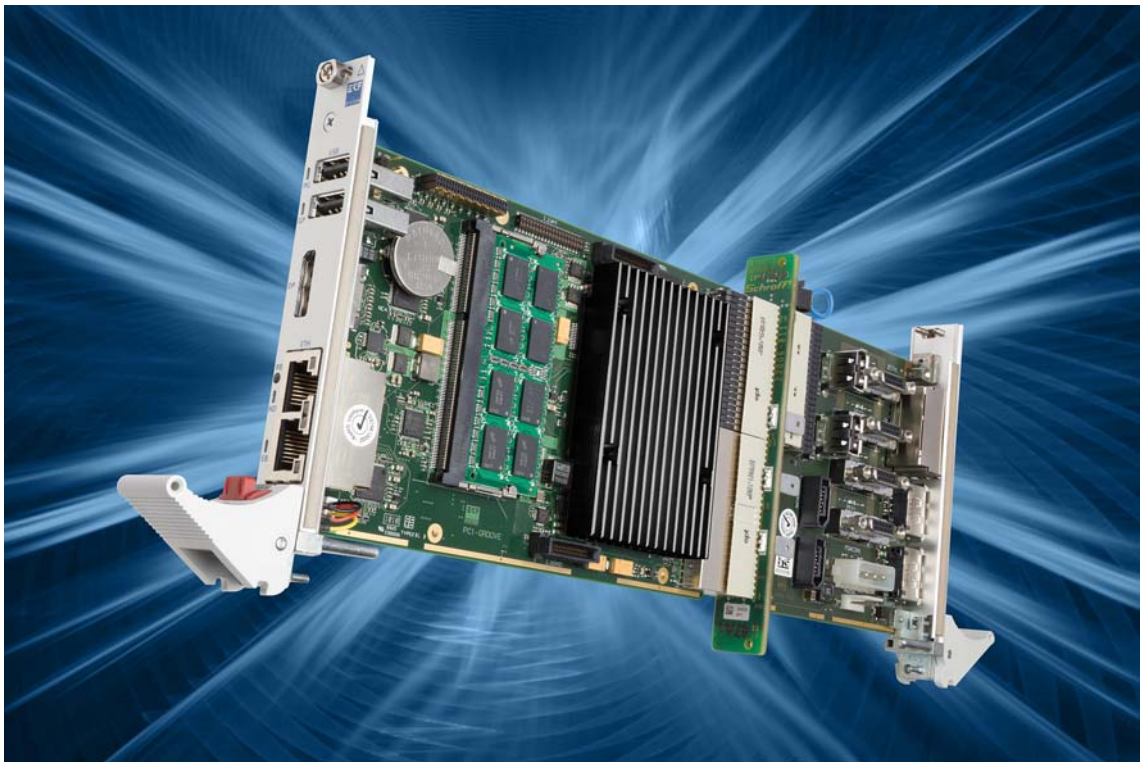


PR1-RIO w. on-Board USB Stick



PR1-RIO w. on-Board PE Cable Connectors

PC1-GROOVE & PR1-RIO



PC1-GROOVE & PR1-RIO

Installing and Replacing Components

Before You Begin

Warnings

The procedures in this chapter assume familiarity with the general terminology associated with industrial electronics and with safety practices and regulatory compliance required for using and modifying electronic equipment. Disconnect the system from its power source and from any telecommunication links, networks or modems before performing any of the procedures described in this chapter. Failure to disconnect power, or telecommunication links before you open the system or perform any procedures can result in personal injury or equipment damage. Some parts of the system can continue to operate even though the power switch is in its off state.

Caution

Electrostatic discharge (ESD) can damage components. Perform the procedures described in this chapter only at an ESD workstation. If such a station is not available, you can provide some ESD protection by wearing an antistatic wrist strap and attaching it to a metal part of the system chassis or board front panel. Store the board only in its original ESD protected packaging. Retain the original packaging (antistatic bag and antistatic box) in case of returning the board to EKF for repair.

Installing the Board

Warning

This procedure should be done only by qualified technical personnel. Disconnect the system from its power source before doing the procedures described here. Failure to disconnect power, or telecommunication links before you open the system or perform any procedures can result in personal injury or equipment damage.

Typically you will perform the following steps:

- Switch off the system, remove the AC power cord
- Attach your antistatic wrist strap to a metallic part of the system 
- Remove the board packaging, be sure to touch the board only at the front panel
- Identify the related *CompactPCI* slot (peripheral slot for I/O boards, system slot for CPU boards, with the system slot typically most right or most left to the backplane)
- Insert card carefully (be sure not to damage components mounted on the bottom side of the board by scratching neighboured front panels)
- A card with onboard connectors requires attachment of associated cabling now
- Lock the ejector lever, fix screws at the front panel (top/bottom)
- Retain original packaging in case of return

Removing the Board

Warning

This procedure should be done only by qualified technical personnel. Disconnect the system from its power source before doing the procedures described here. Failure to disconnect power, or telecommunication links before you open the system or perform any procedures can result in personal injury or equipment damage.

Typically you will perform the following steps:

- Switch off the system, remove the AC power cord
- Attach your antistatic wrist strap to a metallic part of the system
- Identify the board, be sure to touch the board only at the front panel
- unfasten both front panel screws (top/bottom), unlock the ejector lever
- Remove any onboard cabling assembly
- Activate the ejector lever
- Remove the card carefully (be sure not to damage components mounted on the bottom side of the board by scratching neighboured front panels)
- Store board in the original packaging, do not touch any components, hold the board at the front panel only

Warning

Do not expose the card to fire. Battery cells and other components could explode and cause personal injury.

EMC Recommendations

In order to comply with the CE regulations for EMC, it is mandatory to observe the following rules:

- The chassis or rack including other boards in use must comply entirely with CE
- Close all board slots not in use with a blind front panel
- Front panels must be fastened by built-in screws
- Cover any unused front panel mounted connector with a shielding cap
- External communications cable assemblies must be shielded (shield connected only at one end of the cable)
- Use ferrite beads for cabling wherever appropriate
- Some connectors may require additional isolating parts

Reccomended Accessories

Blind CPCI Front Panels	EKF Elektronik	Widths currently available (1HP=5.08mm): with handle 4HP/8HP without handle 2HP/4HP/8HP/10HP/12HP
Ferrit Bead Filters	ARP Datacom, 63115 Dietzenbach	Ordering No. 102 820 (cable diameter 6.5mm) 102 821 (cable diameter 10.0mm) 102 822 (cable diameter 13.0mm)
Metal Shielding Caps	Conec-Polytronic, 59557 Lippstadt	Ordering No. CDFA 09 165 X 13129 X (DB9) CDSFA 15 165 X 12979 X (DB15) CDSFA 25 165 X 12989 X (DB25)

Installing or Replacing the Memory Module

Note: If you decide to replace the memory, observe the precautions in 'Before You Begin'

By default, the PC1-GROOVE is delivered with onboard memory only, the SODIMM DDR3 SDRAM socket is empty.

To expand the memory a DDR3 SDRAM SODIMM module may be inserted in the socket SODM1. It is necessary to use an SODIMM that provide *Serial Presence Detect* (SPD) information, since this allows the chipset to accurately configure the memory settings for optimum performance.

A replacement memory module must match the 204-pin SODIMM form factor (known from Notebook PCs), DDR3, V_{CC}=1.5V, PC3-6400/PC3-8500 (800/1066MHz), on-die termination (ODT), unbuffered, non-ECC style. Suitable modules are available up to 4GB. The Core™ i7 memory controller supports modules of up to a maximum of 16 address lines (A0...A15). Memory modules organized by more than 16 address lines are not suitable.

Replacement of the Battery

When your system is turned off, a battery maintains the voltage to run the time-of-day clock and to keep the values in the CMOS RAM. The battery should last during the lifetime of the PC1-GROOVE. For replacement, the old battery must be unsoldered, and the new one soldered. We suggest that you send back the board to EKF for battery replacement.

Warning

Danger of explosion if the battery is incorrectly replaced or shorted. Replace only with the same or equivalent type. Do not expose a battery to fire.

Technical Reference

Local PCI Devices

The following table shows the on-board PCI devices and their location within the PCI configuration space. These devices consist of some locale controllers and several devices within the Intel 5 series express chip set.

Bus Number	Device Number	Function Number	Vendor ID	Device ID	Description
0	0	0	0x8086	0x0044	Host Bridge/DRAM Controller
0	1	0	0x8086	0x0045	Host-PCIe Bridge
0	2	0	0x8086	0x0046	Internal Graphics Device
0	22	0	0x8086	0x3B64	ME Interface #1
0	22	1	0x8086	0x3B65	ME Interface #2
0	22	2	0x8086	0x3B66	ME IDE Redirection
0	22	3	0x8086	0x3B67	Keyboard Text Redirection
0	25	0	0x8086	0x10EA	PCH Gigabit LAN NC1 (82577)
0	26	0	0x8086	0x3B3C	USB 2.0 EHCI Controller #2
0	27	0	0x8086	0x3B56	Intel High Definition Audio
0	28	0	0x8086	0x3B42	PCI Express Port 1
0	28	1	0x8086	0x3B44	PCI Express Port 2
0	28	2	0x8086	0x3B46	PCI Express Port 3
0	28	3	0x8086	0x3B48	PCI Express Port 4
0	28	4	0x8086	0x3B4A	PCI Express Port 5
0	28	5	0x8086	0x3B4C	PCI Express Port 6
0	28	6	0x8086	0x3B4E	PCI Express Port 7
0	28	7	0x8086	0x3B50	PCI Express Port 8
0	29	0	0x8086	0x3B34	USB 2.0 EHCI Controller #1
0	30	0	0x8086	0x244E	DMI-to-PCI Bridge
0	31	0	0x8086	0x3B07	LPC Bridge
0	31	2	0x8086	0x3B28 0x3B2F 0x3B2C	SATA: Non-AHCI/RAID [1] SATA: AHCI Mode [1] SATA: RAID 0/1/5/10 Mode [1]
0	31	3	0x8086	0x3B30	SMBus Controller
0	31	5	0x8086	0x3B2D	SATA Controller #2
0	31	6	0x8086	0x3B32	Thermal Controller
1 [2]	0	0	0x10B5	0x8614	PCIe Switch (PEX8614)
2 [2]	0	0	0x197B	0x2363 0x2362	PCIe-SATA-Bridge (JMB362 Rev. A) PCIe-SATA-Bridge (JMB362 Rev. C)
3 [2]	0	0	0x8086	0x10D3	Ethernet Controller NC2 (82574)

[1] Depends on BIOS settings.
[2] Bus number can vary depending on the PCI enumeration schema implemented in BIOS.

Local SMB Devices

The PC1-GROOVE contains a few devices that are reachable via the System Management Bus (SMBus). These are the clock generation chip, the SPD EEPROMs for the onboard memory channel or located on the SODIMM memory module, a general purpose serial EEPROM and a supply voltage and temperature controlling device in particular. Other devices could be connected to the SMBus via the *CompactPCI* signals IPMB SCL (J1 B17) and IPMB SDA (J1 C17) or pins 29/30 of the expansion connectors J-EXPT/J-EXPB.

Address	Description
0x58	Hardware Monitor/CPU Temperature Sensor (LM87)
0xA0	SPD of Onboard Memory
0xA4	SPD of SODIMM
0xAE	General Purpose EEPROM
0xD2	Main Clock Generation (CK-505)

Hardware Monitor LM87

Located on the SMBus the PC1-GROOVE offers a hardware monitor of type LM87/NSC. This device is capable to observe board and onboard memory temperatures as well as several supply voltages generated on the board with a resolution of 8 bit. The following table shows the mapping of the voltage inputs of the LM87 to the corresponding supply voltages of the PC1-GROOVE:

Input	Source	Resolution [mV]	Register
AIN1	CPU Core Voltage	9.8	0x28
AIN2	Graphics Core Voltage	9.8	0x29
VCCP1	+1.5V	14.1	0x21
VCCP2/D2-	+1.8V	14.1	0x25
+2.5V/D2+	+1.05V	13	0x20
+3.3V	+3.3V	17.2	0x22
+5V	+5V	26	0x23
+12V	+10V	62.5	0x24

Beside the continuous measuring of temperatures and voltages the LM87 may compare these values against programmable upper and lower boundaries. As soon as a measurement violates the allowed value, the LM87 may request an interrupt via the GPI13 of the PCH.

GPIO Usage

GPIO Usage PCH

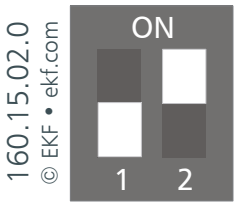
PC1-GROOVE GPIO Usage PCH QM57				
GPIO	Type	Tol.	Function	Description
GPIO 0	I	3.3V	THRM_ALERT#	Monitoring of processor PROCHOT#
GPIO 1	I	3.3V	EXP_SMI#	Expansion Interface SMI Request (J-EXP Pin 15)
GPIO 2	I	5V	CPCI_INTP	CompactPCI Interrupt Request Line INTP
GPIO 3	I	5V	CPCI_ENUM#	CompactPCI System Enumeration Line ENUM#
GPIO 4	I	5V	CPCI_FAL#	CompactPCI Power Failure Line FAL#
GPIO 5	I	5V	CPCI_DEG#	CompactPCI Power Degeneration Line DEG#
GPIO 6	O	3.3V	CPCI_INTS_EN	Connect SERIRQ to CompactPCI Line INTS LOW: SERIRQ disconnected from INTS HIGH: SERIRQ connected to INTS
GPIO 7	I	3.3V	CPCI_SYSEN#	Sense CompactPCI System Slot Enable Line SYSEN#
GPIO 8	O	3.3V	N/A	Not used on PC1 (left NC)
GPIO 9	I	3.3V	USB_OC5#	USB HSE Port #2 Overcurrent Detect
GPIO 10	I	3.3V	USB_OC6#	USB HSE Port #3 or #4 Overcurrent Detect
GPIO 11	I	3.3V	GP_JUMP#	Reset UEFI BIOS Setup to Factory Defaults, Jumper P-GP
GPIO 12	O	3.3V	NC1_ENABLE	Enable Ethernet Controller NC2
GPIO 13	I	3.3V	HM_INT#	Hardware Monitor LM87 Interrupt Line
GPIO 14	I	3.3V	USB_OC7#	USB Front Panel Upper Port Overcurrent Detect
GPIO 15	O	3.3V	N/A	Not used on PC1 (pulled via resistor to +3.3V)
GPIO 16	I	3.3V	N/A	Not used on PC1 (pulled via resistor to +3.3V)
GPIO 17	O	3.3V	CPCI_CLKEN	Enable CompactPCI Clock Buffer
GPIO 18	O	3.3V	GP_LED_RED	General Purpose LED Control (via PLD)
GPIO 19	O	3.3V	PLD_SCL	Local Option Reg Interface (within PLD)
GPIO 20	O	3.3V	SE_SYS_WP	General Purpose Serial EEPROM Write Protection
GPIO 21	O	3.3V	PLD_SDA	Local Option Reg Interface (within PLD)
GPIO 22	O	3.3V	SCLOCK	Serial GPIO Bus CLOCK (J2: SATA_SC)
GPIO 23	I	3.3V	LPC_DRQEXP#	Expansion Interface LPC DMA Request Line
GPIO 24	O	3.3V	USB_POWEN1#	USB Front Panel Upper Port Power Enable
GPIO 25	I	3.3V	N/A	Not used on PC1 (pulled via resistor to +3.3V)
GPIO 26	I	3.3V	N/A	Not used on PC1 (pulled via resistor to +3.3V)
GPIO 27	O	3.3V	USB_POWEN2#	USB Front Panel Lower Port Power Enable
GPIO 28	O	3.3V	CPCI_SMB_EN	Connect SMBus of CPCI IPMB/J-EXP to local SMBus LOW: IPMB/J-EXP disconnected from SMBus HIGH: IPMB/J-EXP connected to SMBus
GPIO 29	O	3.3V	SLP_LAN#	Multiplexed with SLP_LAN#
GPIO 30	I	3.3V	SUS_PWR_DN_ACK	Not used on PC1 (pulled via resistor to +3.3V)
GPIO 31	I	3.3V	ACPRESENT	Not used on PC1 (pulled via resistor to +3.3V)
GPIO 32	I/O	3.3V	CLKRUN#	Fixed to chipset internal function
GPIO 33	I	3.3V	MFG_JUMP#	Select Manufacturing Mode Jumper P-MFG

PC1-GROOVE GPIO Usage PCH QM57					
GPIO	Type	Tol.	Function	Description	
GPIO 34	O	3.3V	STP_PCI#	Multiplexed with chipset internal function	
GPIO 35-37	I	3.3V	HWREV	GPIO 37/36/35 000 001 ... 111	PCB Revision 0 1 ... 7
GPIO 38	O	3.3V	SLOAD	Serial GPIO Bus LOAD (J2: SATA_SL)	
GPIO 39	O	3.3V	SDATAOUT	Serial GPIO Bus DATAOUT (J2: SATA_SC)	
GPIO 40	I	3.3V	USB_OC1#	USB Front Panel Lower Port Overcurrent Detect	
GPIO 41	O	3.3V	ENABLE_NC3	Enable Ethernet Controller NC3	
GPIO 42	O	3.3V	ENABLE_NC4	Enable Ethernet Controller NC4	
GPIO 43	I	3.3V	USB_OC4#	USB J-HSE Port #1 Overcurrent Detect	
GPIO 44	I	3.3V	N/A	Not used on PC1 (pulled via resistor to +3.3V)	
GPIO 45	I	3.3V	WDOGRST	Last Hardware Reset caused by watchdog	
GPIO 46	I	3.3V	N/A	Not used on PC1 (pulled via resistor to +3.3V)	
GPIO 47	I	3.3V	CPCI_12VOK	CompactPCI +12V Present	
GPIO 48	I	3.3V	N/A	Not used on PC1 (pulled via resistor to +3.3V)	
GPIO 49	I	3.3V	N/A	Not used on PC1 (pulled via resistor to GND)	
GPIO 50	I	5V	CPCI_REQ1#	CompactPCI Bus Request Line CPCI_REQ1#	
GPIO 51	O	3.3V	CPCI_GNT1#	CompactPCI Bus Grant Line CPCI_GNT1#	
GPIO 52	I	5V	CPCI_REQ2#	CompactPCI Bus Request Line CPCI_REQ2#	
GPIO 53	O	3.3V	CPCI_GNT2#	CompactPCI Bus Grant Line CPCI_GNT2#	
GPIO 54	I	5V	CPCI_REQ3#	CompactPCI Bus Request Line CPCI_REQ3#	
GPIO 55	O	3.3V	CPCI_GNT3#	CompactPCI Bus Grant Line CPCI_GNT3#	
GPIO 56	I	3.3V	N/A	Not used on PC1 (pulled via resistor to +3.3V)	
GPIO 57	O	3.3V	ENABLE_NC2	Enable Ethernet Controller NC2	
GPIO 58	I	3.3V	N/A	Not used on PC1 (pulled via resistor to +3.3V)	
GPIO 59	I	3.3V	USB_OC0#	USB Front Panel Upper Port Overcurrent Detect	
GPIO 60	I	3.3V	N/A	Not used on PC1 (pulled via resistor to +3.3V)	
GPIO 61	O	3.3V	N/A	Not used on PC1 (left NC)	
GPIO 62	O	3.3V	SUSCLK	Multiplexed with chipset internal function	
GPIO 63	O	3.3V	SLP_S5#	Multiplexed with chipset internal function	
GPIO 64-67	I	3.3V	BOARD_CFG	Board Configuration Jumpers	
GPIO68-71	N/A	N/A	N/A	Not implemented in PCH QM57	
GPIO 72	I	3.3V	N/A	Not used on PC1 (pulled via resistor to +3.3V)	
GPIO 73	I	3.3V	NC1_CLKREQ#	Multiplexed with chipset internal function	
GPIO 74	I	3.3V	N/A	Not used on PC1 (pulled via resistor to +3.3V)	
GPIO 75	I	3.3V	N/A	Not used on PC1 (pulled via resistor to +3.3V)	

Configuration Jumpers

Configuration Switches PCI Express Link Width (DSW1)

The link width of the PCI Express interfaces attached to the PlusIO interface J2/P2 and the local expansion connector P-PCIE is configurable by two DIP switches (DSW1) located on the backside of the PC1-GROOVE. Note that changes in PCIe link width configuration are honoured by the PC1-GROOVE not before a system reset was performed.



DSW1

DSW1		PCIe Link Width		
1	2	PCIe Switch Upstream	J2/P2 (PlusIO)	J-PCIE
OFF	OFF	4 Lanes	1 Link x 4 Lanes	1 Link x 4 Lanes
ON	OFF	4 Lanes	4 Links x 1 Lane	1 Link x 4 Lanes
OFF	ON	4 Lanes	4 Links x 1 Lane	4 Links x 1 Lane
ON [1)]	ON [1)]	1 Lane	4 Links x 1 Lane	4 Links x 1 Lane

[1)] This setting is not useful and should not be used.

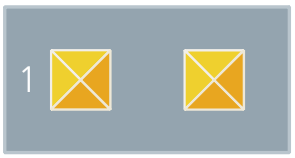
When a port is configured as single link, the PCIe switch may size down the link width to x2 or x1 by auto-negotiation.

The following table shows the factory settings of DSW1 with different side boards mounted to the PC1-GROOVE:

Side Board	DSW1		PCIe Link Width		
	1	2	Upstream	J2/P2 (PlusIO)	J-PCIE
None	OFF	ON	4 Lanes	4 Links x 1 Lane	4 Links x 1 Lane
C23-SATA	OFF	ON	4 Lanes	4 Links x 1 Lane	4 Links x 1 Lane
CCI-RAP	OFF	ON	4 Lanes	4 Links x 1 Lane	4 Links x 1 Lane
CCJ-RHYTHM	ON	OFF	4 Lanes	4 Links x 1 Lane	1 Link x 4 Lanes
CCK-MARIMBA	ON	OFF	4 Lanes	4 Links x 1 Lane	1 Link x 4 Lanes
CCL-CAPELLA	ON	OFF	4 Lanes	4 Links x 1 Lane	1 Link x 4 Lanes
CCO-CONCERT	OFF	ON	4 Lanes	4 Links x 1 Lane	4 Links x 1 Lane

Loading UEFI BIOS Setup Defaults (P-GP)

The jumper P-GP is used to reset the UEFI BIOS configuration settings to a default state. The UEFI BIOS on PC1-GROOVE stores most of its settings in an area within the BIOS flash, e.g. the actual boot devices. Using the jumper P-GP is only necessary, if it is not possible to enter the setup of the BIOS. To reset the settings mount a jumper on P-GP and perform a system reset. As long as the jumper is stuffed the BIOS will use the default configuration values after any system reset. To get normal operation again, the jumper has to be removed.



P-GP

P-GP	Function
Jumper OFF [1)]	Normal operation
Jumper ON	BIOS configuration reset performed

[1)] This setting is the factory default.

Manufacturer Mode Jumper (P-MFG)

The jumper P-MFG is used to bring the board into the manufacturer mode. This is necessary only on board production time and should not used by customers. For normal operation the jumper should be removed.

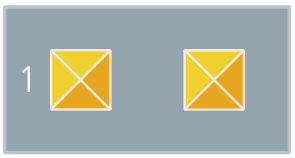
P-MFG

P-MFG	Function
Jumper OFF [1)]	Normal Mode
Jumper ON	Manufacturer Mode

[1)] This setting is the factory default.
[2)] P-MFG is not stuffed.

Reset Jumper PCH RTC Core (P-RTC)

The jumper P-RTC is used to reset the battery backed core of the PCH. This effects some registers within the PCHs RTC core that are important before the CPU starts its work after a system reset. Note that P-RTC will neither set UEFI BIOS Setup to EKF Factory Defaults nor resets the real time clock. To reset the RTC core the board must be removed from the system rack. Short-circuit the pins of P-RTC for about 1 sec. After that reinstall the board to the system and switch on the power. It is important to accomplish the RTC reset while the board has no power.



P-RTC

P-RTC	Function
Jumper OFF [1)]	No RTC reset performed
Jumper ON	RTC reset performed

[1)] This setting is the factory default.
[2)] P-RTC is not stuffed.

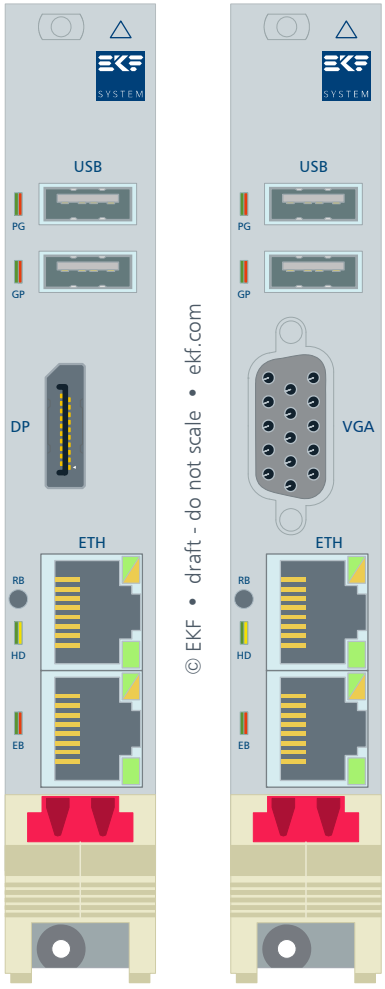
Connectors

Caution

Some of the internal connectors provide operating voltage (3.3V and 5V) to devices inside the system chassis, such as internal peripherals. Not all of these connectors are overcurrent protected. Do not use these internal connectors for powering devices external to the computer chassis. A fault in the load presented by the external devices could cause damage to the board, the interconnecting cable and the external devices themselves.

Front Panel Connectors

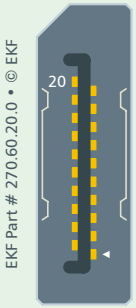
Typical PC1-GROOVE Front Panel Elements



PC1-GROOVE DisplayPort

PC1-GROOVE VGA

DisplayPort Monitor Connector J-DP

DisplayPort J-DP				
	20	PWR [1]	19	RETURN (GND)
	18	HPD	17	AUX_CH(N)
	16	GND	15	AUX_CH(P)
	14	CONFIG2 (GND)	13	CONFIG1
	12	LANE3(N)	11	GND
	10	LANE3(P)	9	LANE2(N)
	8	GND	7	LANE2(P)
	6	LANE1(N)	5	GND
	4	LANE1(P)	3	LANE0(N)
	2	GND	1	LANE0(P)

[1] +3.3V protected by a PolySwitch Fuse 0.5A. This voltage is switched on in S0 state only.

For attachment of either a classic style analog RGB monitor or DVI type display to the J-DP receptacle, there are both adapters and also adapter cables available, from DisplayPort to the VGA or DVI connector.

Plug Style Adapter

Plug Style DP to DVI Adapter

Cable Adapter DP to DVI

Cable Adapter DP to VGA

Specified by the VESA DisplayPort connector standard is a dedicated power pin 20 (+3.3V 0.5A). Both the GPU (source side) and a DP monitor (sink side) must provide power via this pin. A VESA specified DisplayPort cable however must not connect the pins 20 of both cable ends, in order to avoid a back driving conflict. Unfortunately there are cable assemblies available with pin 20 passed through, with unpredictable results on the system behaviour. Before ordering DP cable assemblies, verify the associated wiring diagram.

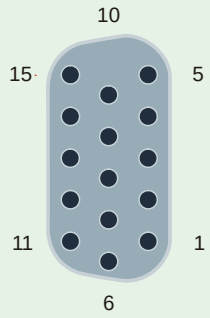
Sample VESA Compliant DisplayPort Cable Assemblies 2.0m Plug to Plug, w. Latches • EKF Part. #270.66.1.02.0	
Manhattan	307116, 391931
Molex	68783-0007
TE (Tyco)	2040687-2, 2040638-2

A secondary DiplayPort video output is available with the mezzanine side card PCS-BALLET, for operation of two independent monitors (e.g. Extended Desktop).

PC1-GROOVE 12HP Assembly w. PCS-BALLET & C32-FIO

Video Monitor Connector J-VGA

As an option, the PC1-GROOVE can be equipped with a legacy VGA connector (High-Density D-Sub 15-position female connector). The connector J-VGA replaces the J-DP receptacle, and the digital DisplayPort video interface therefore is not available concurrently with this option.

J-VGA (Option)		
	1	RED
	2	GREEN
	3	BLUE
	4	NC
	5	GND
	6	GND
	7	GND
	8	GND
	9	DDC_POW [1)]
	10	GND
	11	NC
	12	VGA_DDC_SDA
	13	HSYNC
	14	VSYNC
	15	VGA_DDC_SCL

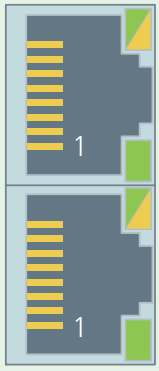
[1)] +5V protected by a PolySwitch Fuse 0.5A. This power rail is switched on in S0 state only.

USB Connectors

USB Ports 1/2 (J-USB1/J-USB2)		
 #270.20.04.2 ©EKF • ekf.com	1	POW [1]
	2	USB DATA (N)
	3	USB DATA (P)
	4	GND

[1] +5V protected by an Electronic Fuse 0.5A. Power rail may be switched off by software independently for each port.

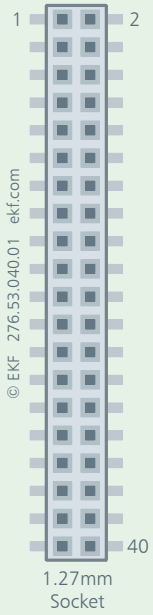
Ethernet Connectors

Gigabit Ethernet Ports 1/2 (J-ETH, RJ45)			
 270.02.08.5	Port 1	1	NC1_MDX0+
		2	NC1_MDX0-
		3	NC1_MDX1+
		4	NC1_MDX2+
		5	NC1_MDX2-
		6	NC1_MDX1-
		7	NC1_MDX3+
		8	NC1_MDX3-
	Port 2	1	NC2_MDX0+
		2	NC2_MDX0-
		3	NC2_MDX1+
		4	NC2_MDX2+
		5	NC2_MDX2-
		6	NC2_MDX1-
		7	NC2_MDX3+
		8	NC2_MDX3-

The lower green LED indicates LINK established when continuously on, and data transfer (activity) when blinking. If the lower green LED is permanently off, no LINK is established. The upper green/yellow dual-LED signals the link speed 1Gbit/s when lit yellow, 100Mbit/s when lit green, and 10Mbit/s when off.

Internal Connectors

Expansion Interface Header J-EXP



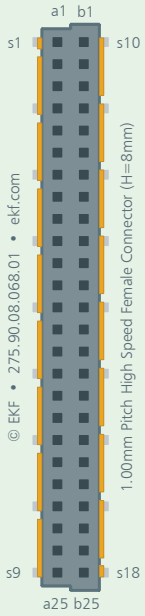
J-EXPT (J-EXPB optinal)			
GND	1	2	+3.3V [1]
PCI_CLK (33MHz)	3	4	PLTRST#
LPC_AD0	5	6	LPC_AD1
LPC_AD2	7	8	LPC_AD3
LPC_FRM#	9	10	LPC_DRQ#
GND	11	12	+3.3V [1]
SERIRQ	13	14	EXP_PME#
EXP_SMI#	15	16	SIO_CLK (14.3MHz)
FWH_ID0	17	18	FWH_INIT#
PCH_RCIN#	19	20	PCH_A20GATE
GND	21	22	+5V [1]
USB_EXP_P2-	23	24	USB_EXP_P1-
USB_EXP_P2+	25	26	USB_EXP_P1+
USB_EXP_OC#	27	28	H_DBRESET#
EXP_SCL [2]	29	30	EXP_SDA [2]
GND	31	32	+5V [1]
HDA_SDOUT	33	34	HDA_SDIN0
HDA_RST#/CL_RST# [3]	35	36	HDA_SYNC
HDA_BITCLK/CL_CLK [3]	37	38	HDA_SDIN1/CL_DATA [3]
SPEAKER	39	40	+12V [4]

[1] Power rail switched on in state S0 only.
[2] Connected to SMBus via switch, isolated after PCI reset.
[3] Stuffing option, default is the HDA option.
[4] Unswitched power rail (switched on always).

The expansion interface header footprint is available on both sides of the board, top (J-EXPT) and bottom (J-EXPB). Nevertheless the bottom side connector is stuffed only on customers request.

WARNING: Neither the +3.3V pin, nor the +5V pin, nor the +12V pin are protected against a short circuit situation! This connector therefore should be used only for attachment of an expansion board. The maximum current flowing across these pins should be limited to 2A per power rail.

High Speed Expansion Connector J-HSE



High Speed Expansion J-HSE			
GND	a1	b1	GND
SATA_HSE1_TXP [3) 5)]	a2	b2	SATA_HSE3_TXP [4) 5) 6)]
SATA_HSE1_TXN [3) 5)]	a3	b3	SATA_HSE3_TXN [4) 5) 6)]
GND	a4	b4	GND
SATA_HSE1_RXN [3) 5)]	a5	b5	SATA_HSE3_RXN [4) 5) 6)]
SATA_HSE1_RXP [3) 5)]	a6	b6	SATA_HSE3_RXP [4) 5) 6)]
GND	a7	b7	GND
SATA_HSE2_TXP [4) 5) 6)]	a8	b8	SATA_HSE4_TXP [3) 5) 6)]
SATA_HSE2_TXN [4) 5) 6)]	a9	b9	SATA_HSE4_TXN [3) 5) 6)]
GND	a10	b10	GND
SATA_HSE2_RXN [4) 5) 6)]	a11	b11	SATA_HSE4_RXN [3) 5) 6)]
SATA_HSE2_RXP [4) 5) 6)]	a12	b12	SATA_HSE4_RXP [3) 5) 6)]
GND	a13	b13	GND
USB_HSE1_P	a14	b14	USB_HSE3_P
USB_HSE1_N	a15	b15	USB_HSE3_N
GND	a16	b16	GND
USB_HSE2_P	a17	b17	USB_HSE4_P
USB_HSE2_N	a18	b18	USB_HSE4_N
GND	a19	b19	GND
USB_HSE1_OC#	a20	b20	USB_HSE34_OC#
USB_HSE2_OC#	a21	b21	USB_HSE34_OC#
+3.3VS [1)]	a22	b22	+5VS [1)]
+3.3VS [1)]	a23	b23	+5VS [1)]
+3.3VA [2)]	a24	b24	+5VA [2)]
+12VA [2)]	a25	b25	*RSVD*

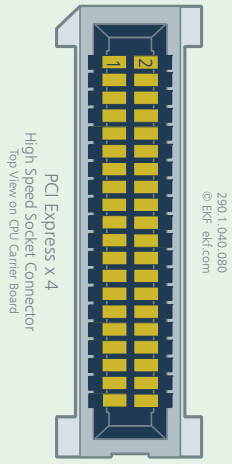
1) Power rail switched on in state S0 only.
2) Power rail switched on with system power.
3) This SATA channel is derived from the PCH.
4) This SATA channel is derived from the JMB362.
5) All TX/RX designations with respect to SATA controller.
6) The SATA Port assignment PCH/JMB362 has been changed in Revision 1 of PC1-GROOVE.

WARNING: Neither the +3.3V pins, nor the +5V pins, nor the +12VA pin are protected against a short circuit situation! This connector therefore should be used only for attachment of the C40-SCFA adapter or an expansion board. The maximum current flowing across these pins should be limited to 2A per power rail.

C47-MSATA • mSATA Mezzanine Module Based on HSE Connector

C48-M2 • M.2 Mezzanine Module Based on HSE Connector

PCI Express Expansion Header J-PCIE

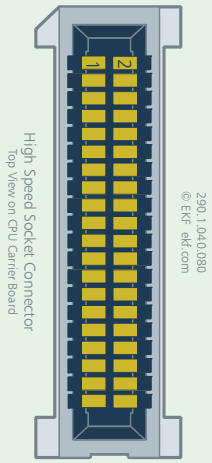


J-PCIE			
GND	1	2	GND
+5V [1]	3	4	+3.3V [1]
+5V [1]	5	6	+3.3V [1]
GND	7	8	GND
PE_CLKP	9	10	PLTRST#
PE_CLKN	11	12	PE_WAKE#
GND	13	14	GND
PE_1TP	15	16	PE_1RP
PE_1TN	17	18	PE_1RN
GND	19	20	GND
GND	21	22	GND
PE_2TP	23	24	PE_2RP
PE_2TN	25	26	PE_2RN
GND	27	28	GND
PE_3TP	29	30	PE_3RP
PE_3TN	31	32	PE_3RN
GND	33	34	GND
PE_4TP	35	36	PE_4RP
PE_4TN	37	38	PE_4RN
GND	39	40	GND

[1] Power rail switched on in state S0 only.

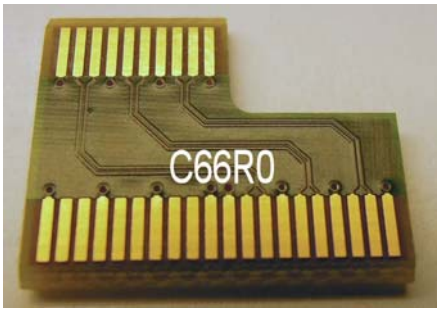
WARNING: Neither the +3.3V pin, nor the +5V pin are protected against a short circuit situation! The maximum current flowing across these pins should be limited to 2A per power rail.

SDVO2 Expansion Header J-SDVO2

J-SDVO2				
	GND	1	2	GND
	SDVO_RED+	3	4	SDVO_CLK+
	SDVO_RED-	5	6	SDVO_CLK-
	GND	7	8	GND
	SDVO_GREEN+	9	10	SDVO_INT+
	SDVO_GREEN-	11	12	SDVO_INT-
	GND	13	14	GND
	SDVO_BLUE+	15	16	SDVO_CTR_CLK
	SDVO_BLUE-	17	18	SDVO_CTR_DATA
	GND	19	20	GND
	GND	21	22	GND
	DP_LANE0(P)	23	24	DP_LANE3(P)
	DP_LANE0(N)	25	26	DP_LANE3(N)
	GND	27	28	GND
	DP_LANE1(P)	29	30	DP_AUX(P)
	DP_LANE1(N)	31	32	DP_AUX(N)
	GND	33	34	GND
	DP_LANE2(P)	35	36	DP_HDP
	DP_LANE2(N)	37	38	DP_CDATA
	GND	39	40	GND

A suitable mating strip line PCB must be used, depending whether the DVI or DisplayPort video output is provided on the particular mezzanine side card. With respect to the CCO-CONCERT (DVI) the C26 intermediate PCB must be used. For the PCS-BALLET (DisplayPort) however, the C66 spacer card is required.

C26 use with
CCO-CONCERT (DVI)



C66 use with
PCS-BALLET (DP)

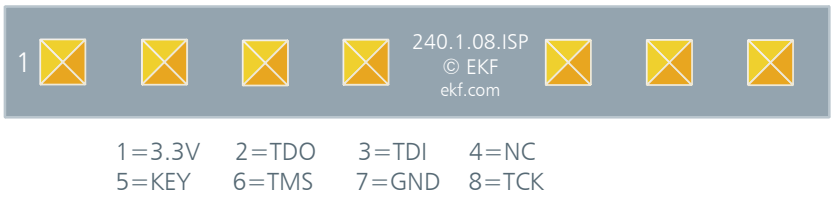
Front Panel Handle Microswitch Header P-FPH

The jumper P-FPH is used to perform power button events. By default P-FPH is connected with a short cable to a micro switch located within the front panel handle. The switch performs power button events by short-circuiting the pins 1 and 3 of P-FPH.

1=PWRBTN# 2=NC 3=GND

P-FPH

PLD Programming Header P-ISP



P-ISP

Note: P-ISP is not stuffed. Its footprint is situated at the bottom side of the board.

Processor Debug Header XDP1

XDP1			
1	PREQ#	BCLKN/HOOK5	13
2	PRDY#	VCC	14
3	GND	RST#/HOOK6	15
4	OBSDATA0 (NC)	DBR#/HOOK7	16
5	OBSDATA1 (NC)	GND	17
6	GND	TDO	18
7	OBSDATA2 (NC)	TRST#	19
8	OBSDATA3 (NC)	TDI	20
9	GND	TMS	21
10	PWRGD/HOOK0	TCK1 (NC)	22
11	HOOK2 (NC)	GND	23
12	BCLKP/HOOK4	TCK	24

Note: XDP1 is not stuffed. Its footprint is situated at the bottom side of the board.

CompactPCI J1

J1	A	B	C	D	E
25	5V	*REQ64#* [2]	ENUM# [1]	3.3V	5V
24	AD1	5V	V(I/O)	AD0	*ACK64#* [2]
23	3.3V	AD4	AD3	5V	AD2
22	AD7	GND	3.3V	AD6	AD5
21	3.3V	AD9	AD8	GND/M66EN [3]	C/BE0#
20	AD12	GND	V(I/O)	AD11	AD10
19	3.3V	AD15	AD14	GND	AD13
18	SERR# [1]	GND	3.3V	PAR	C/BE1#
17	3.3V	IPMB SCL [4]	IPMB SDA [4]	GND	PERR# [1]
16	DEVSEL# [1]	GND	V(I/O)	STOP# [1]	LOCK# [1]
15	3.3V	FRAME# [1]	IRDY# [1]	BD_SEL# [7]	TRDY# [1]
14	KEY AREA				
13					
12					
11	AD18	AD17	AD16	GND	C/BE2#
10	AD21	GND	3.3V	AD20	AD19
9	C/BE3#	GND	AD23	GND	AD22
8	AD26	GND	V(I/O)	AD25	AD24
7	AD30	AD29	AD28	GND	AD27
6	REQ# [1]	GND	3.3V	CLK	AD31
5	*BRSVP1A5* [5]	*BRSVP1B5* [5]	RST#	GND	GNT#
4	IPMB PWR	GND	V(I/O)	INTP [1]	INTS [1]
3	INTA# [1]	INTB# [1]	INTC# [1]	5V	INTD# [1]
2	*TCK* [5]	5V	*TMS* [5]	*TDO* [5]	*TDI* [5]
1	5V	-12V [6]	*TRST#* [5]	+12V	5V

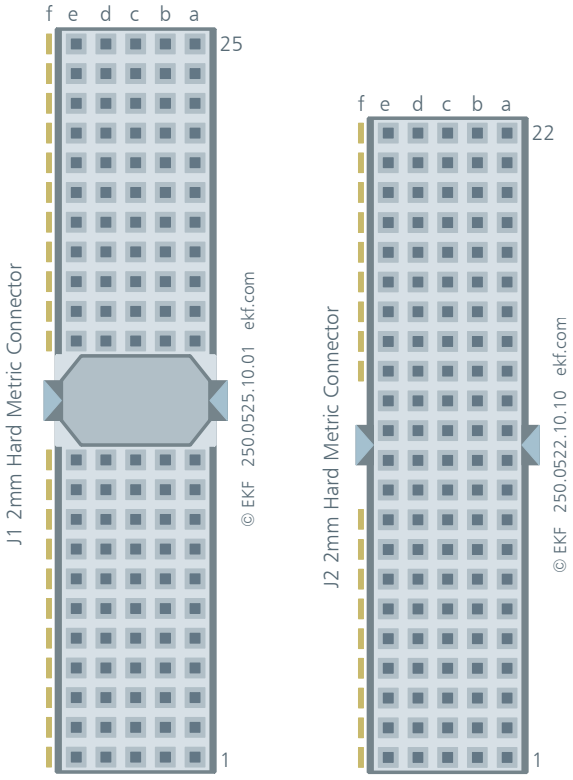
1) This pin is pulled up with 1kΩ to V(I/O). Other pull up resistor values (e.g. 2.7kΩ for V(I/O)=+3.3V) are available on request.
2) This pin is not used on PC1-GROOVE, but pulled up with 1kΩ to V(I/O). Other pull up resistor values on request.
3) This pin is fixed to GND on PC1-GROOVE to force 33MHz operation since 66MHz operation is not supported.
4) This pin is pulled up with 3.0k to J1 pin A4.
5) This pin is not connected.
6) This pin is connected to a decoupling capacitor only and not used on PC1-GROOVE.
7) This pin is connected to power sequencing logic and should pulled low for normal operation.

CompactPCI J2 (PlusIO)

This connector is a high speed UHM connector, suitable for Gigabit Serial I/O
Refer also to PICMG® 2.30 CompactPCI® PlusIO Specification

J2	A	B	C	D	E
22	*GA4* [2]	*GA3* [2]	*GA2* [2]	*GA1* [2]	*GA0* [2]
21	CLK6	GND	2_ETH_B+ *RSV*	1_ETH_D+ *RSV*	1_ETH_B+ *RSV*
20	CLK5	GND	2_ETH_B- *RSV*	1_ETH_D- *GND*	1_ETH_B- *RSV*
19	GND	GND	2_ETH_A+ *RSV*	1_ETH_C+ *RSV*	1_ETH_A+ *RSV*
18	2_ETH_D+ *BRSVP2A18*	2_ETH_C+ *BRSVP2B18*	2_ETH_A- *BRSVP2C18*	1_ETH_C- *GND*	1_ETH_A- *BRSVP2E18*
17	2_ETH_D- *BRSVP2A17*	2_ETH_C- *GND*	PRST# [1]	REQ6# [1]	GNT6#
16	4_PE_CLK- *BRSVP2A16*	2_PE_CLK+ *BRSVP2B16*	DEG# [1]	GND	reserved [2] *BRSVP2E16*
15	4_PE_CLK+ *BRSVP2A15*	2_PE_CLK- *GND*	FAL# [1]	REQ5# [1]	GNT5#
14	3_PE_CLK- *AD35*	1_PE_CLK+ *AD34*	4_PE_CLKE# *AD33*	SATA_SCL *GND*	reserved [2] *AD32*
13	3_PE_CLK+ *AD38* [1]	1_PE_CLK- *GND*	3_PE_CLKE# *V(I/O)*	SATA_SDO *AD37*	SATA_SL *AD36*
12	4_PE_RX00+ *AD42*	1_PE_CLKE# *AD41*	2_PE_CLKE# *AD40*	SATA_SDI [2] *GND*	4_SATA_RX+ *AD39*
11	4_PE_RX00- *AD45*	4_PE_TX00+ *GND*	4_USB2+ *V(I/O)*	4_SATA_TX+ *AD44*	4_SATA_RX- *AD43*
10	3_PE_RX00+ *AD49*	4_PE_TX00- *AD48*	4_USB2- *AD47*	4_SATA_TX- *GND*	3_SATA_RX+ *AD46*
9	3_PE_RX00- *AD52*	3_PE_TX00+ *GND*	3_USB2+ *V(I/O)*	3_SATA_TX+ *AD51*	3_SATA_RX- *AD50*
8	2_PE_RX00+ *AD56*	3_PE_TX00- *AD55*	3_USB2- *AD54*	3_SATA_TX- *GND*	2_SATA_RX+ *AD53*
7	2_PE_RX00- *AD59*	2_PE_TX00+ *GND*	2_USB2+ *V(I/O)*	2_SATA_TX+ *AD58*	2_SATA_RX- *AD57*
6	1_PE_RX00+ *AD63*	2_PE_TX00- *AD62*	2_USB2- *AD61*	2_SATA_TX- *GND*	1_SATA_RX+ *AD60*
5	1_PE_RX00- *C/BE5#*	1_PE_TX00+ 64EN#	1_USB2+ *V(I/O)*	1_SATA_TX+ *C/BE4#*	1_SATA_RX- *PAR64*
4	V(I/O)	1_PE_TX00- *BRSVP2B4*	1_USB2- *C/BE7#*	1_SATA_TX- *GND*	reserved [2] *C/BE6#*
3	CLK4	GND	GNT3#	REQ4# [1]	GNT4#
2	CLK2	CLK3	SYSEN# [3]	GNT2#	REQ3# [1]
1	CLK1	GND	REQ1# [1]	GNT1#	REQ2# [1]

1) This pin is pulled up with 1kΩ to V(I/O). Alternate pull up resistor values (e.g. 2.7kΩ for V(I/O)=+3.3V) are available on request.
2) This pin is not connected.
3) This pin is pulled up with 10kΩ to +3.3V.
4) *Pin positions printed italic: 64-bit system slot signals (for reference only).*
5) Pin positions printed blue: PlusIO options.

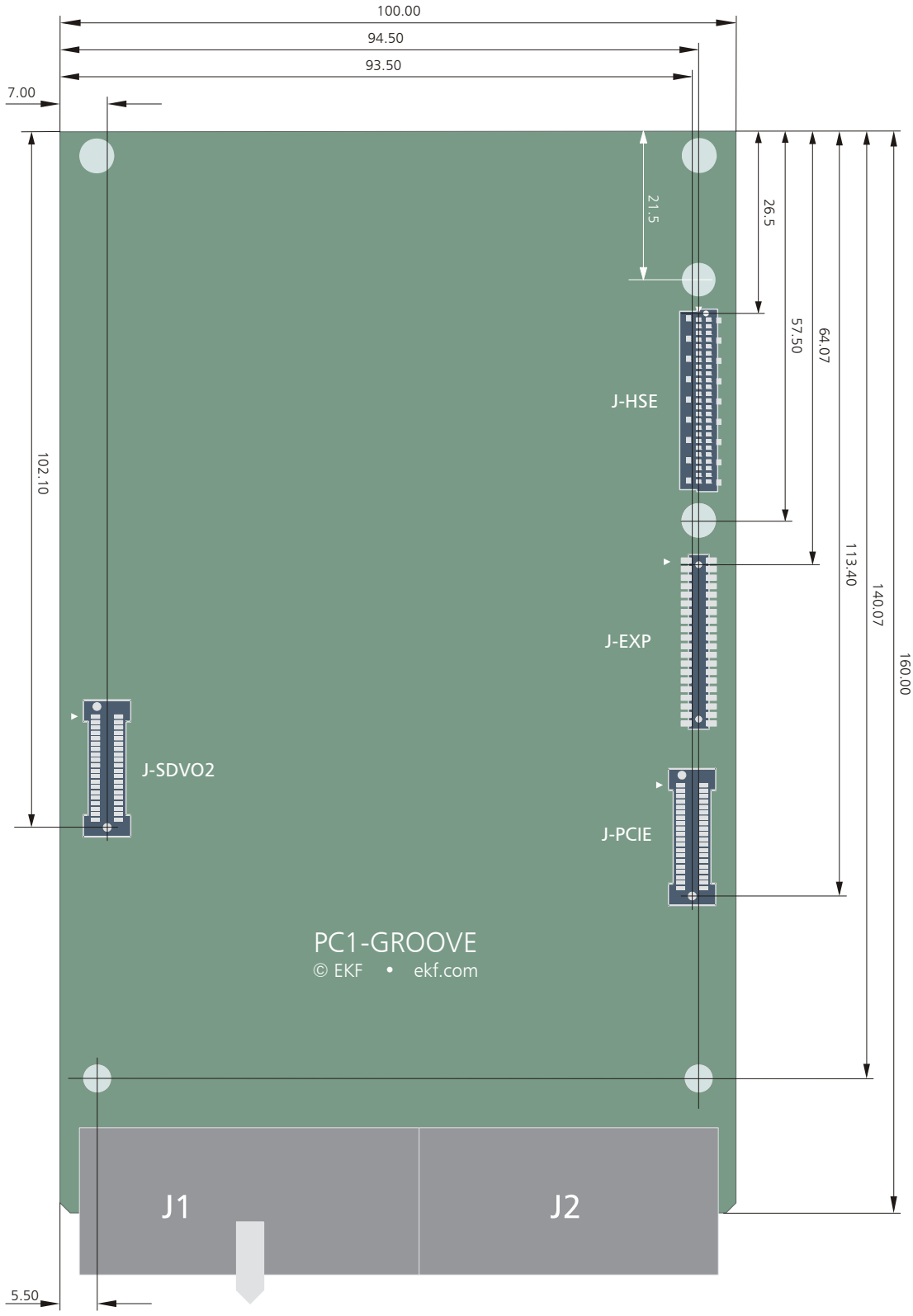


J2 UHM (Top)
J1 (Bottom)

Appendix

Mechanical Drawings

The following drawing shows the positions of mounting holes and expansion connectors on the PC1-GROOVE.



Small Industrial Systems

Small Industrial Systems

Rugged Industrial Systerms

Rugged Industrial Systems

Full Size Industrial System

Custom Specific System

C40-SCFA CompactFlash Module

C41-CFAST CFast Module

C42-SATA 1.8-Inch Micro SATA Module

C43-SATA Internal SATA Connector Module

C47-MSATA Dual mSATA SSD Module

Custom Specific Front Panel Solutions Available

PC1-GROOVE

PC1-GROOVE with C47-MSATA RAID Storage Mezzanine Module

PC1-GROOVE • PCS-BALLET Side Card (8HP Assembly)

PC1-GROOVE • PCS-BALLET Side Card (12HP Assembly)

PC1-GROOVE w. PCS-BALLET Side Card & C42-SATA Mezzanine

PC1-GROOVE w. PCS-BALLET Side Card & C47-MSATA Mezzanine

EKF Elektronik GmbH
Philipp-Reis-Str. 4 (Haus 1)
Lilienthalstr. 2 (Haus 2)
59065 HAMM
Germany

Phone +49 (0)2381/6890-0
Fax +49 (0)2381/6890-90
Internet www.ekf.com
E-Mail sales@ekf.com