SYSTEM

Product Information

SY7-CYCLONE

CompactPCI® Serial

FPGA Based Universal Networking Platform
PCIe® x4 • 10/20 Port 100BASE-T1 Single Pair Ethernet (SPE)

General

The SY7-CYCLONE is a CompactPCI® Serial peripheral board, equipped with a powerful FPGA, and front panel I/O connectors for 10 x 100BASE-T1 Single Pair Ethernet. With its PCI Express® x4 interface, the Cyclone®-V FPGA can be configured e.g. as Ethernet NIC, switch, router, or gateway. Industrial Ethernet real time protocols and custom specific applications may be integrated. SPE (Single Pair Ethernet) is a new standard for many automotive and industrial applications.

The 5CGXFC7C6F23I7N Cyclone®-V FPGA operates over the industrial temperature range and contains 150K logic elements, and also hard IPs for the PCI Express® controller. In addition to non-volatile I^2C memory, 512MB DDR3L soldered RAM is wired on-board to the Cyclone-V FPGA. The SY7-CYCLONE is equipped with 100BASE-T1 PHYs designed for automotive robustness, supporting a cable length of at least 15m over a single unshielded twisted pair.

Feature Summary

General

- PICMG® CompactPCI® Serial (CPCI-S.0) peripheral slot board(s)
- Single Size Eurocard 3U 4HP 100x160mm^2 (10 x 100BASE-T1 front ports)
- Assembly of two boards 3U 8HP (20 x 100BASE-T1 front ports)
- CompactPCI® Serial backplane connector(s) P1 for up to x4 PCI Express® lanes/link

FPGA

- Intel® (Altera) 5CGXFC7C6F23I7N FPGA
- Hard IP PCI Express® interface
- Industrial temperature range -40°C to +85°C
- Logic elements 150K
- Adaptive logic modules (ALM) 56480
- Register 225920
- Variable-precision DSP blocks 156
- 18 x 18 multiplier 312
- Alternate scalable FPGA devices on request (C4, C5, C9)
- FPGA mezzanine expansion connector for secondary SY7-CYCLONE board

Networking

- 5 x Molex® Mini50 front panel connectors (4-pos., USCAR 050 approved)
- Each connector used for two individual SPE Ethernet ports (pin 1-2, 3-4)
- 10 x 100BASE-T1 Ethernet ports (IEEE 802.3bw)
- 10 x NXP automotive Ethernet PHYs TJA1101
- PHYs wired via RMII I/F to FPGA differential I/O
- FPGA IP based Ethernet MACs (RMII)
- Two boards can be stacked for 20 x 100BASE-T1 Ethernet ports in total

Feature Summary

Applications

- General industrial networking, FPGA programmable
- Automotive test equipment
- Transportation applications
- Ethernet switch and/or Ethernet NIC functionality
- Router, gateway, bridge, firewall, security, camera links
- Real time applications
- Edge computing, IIoT
- Data acquisition, data concentrator, data accelerator
- SPE as superior replacement for RS-485 and CAN

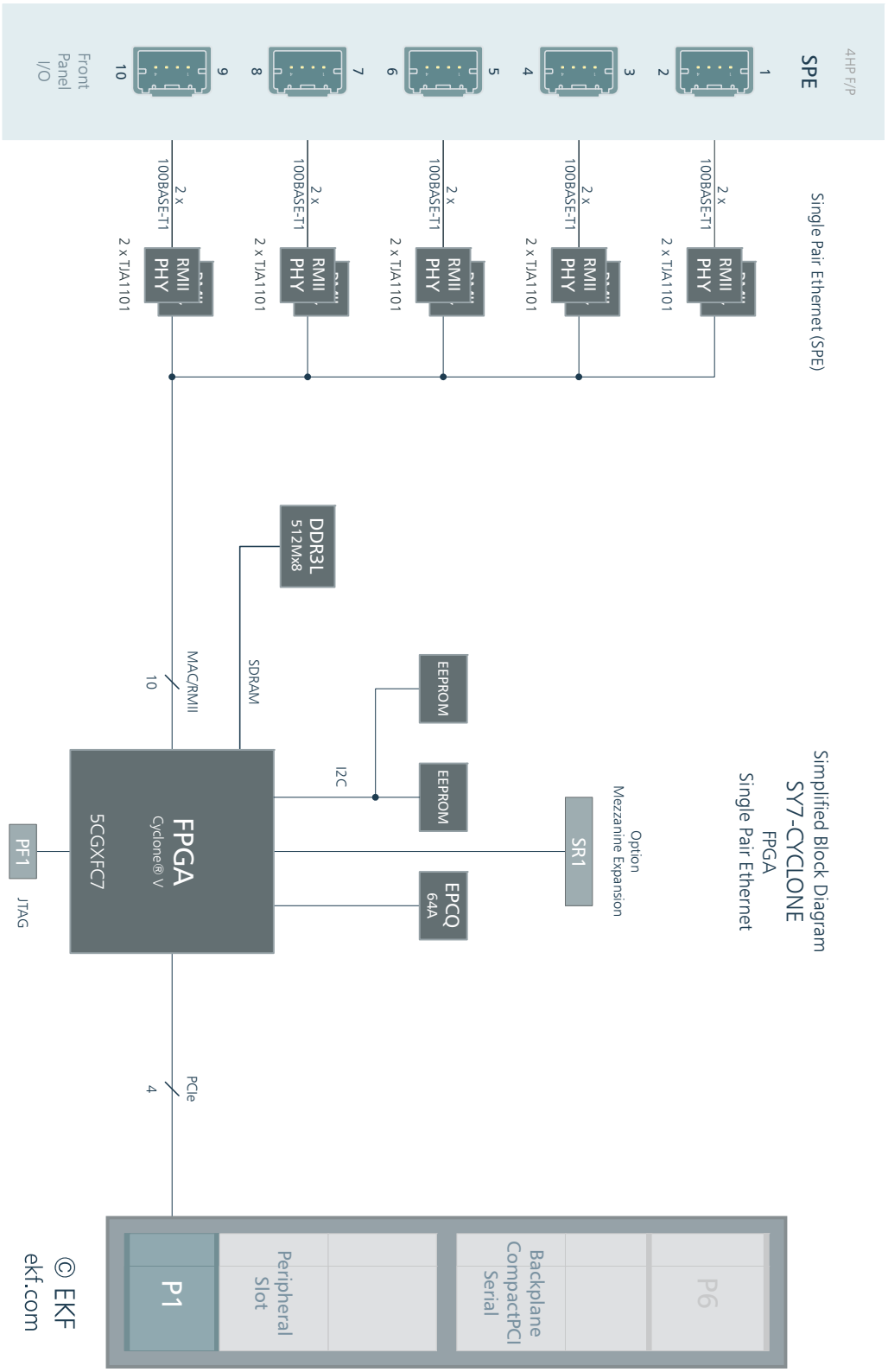
Programming Support

- Reference design available (for Intel® Quartus® Prime design software)
- Linux test tool available
- Custom specific FPGA programming on request

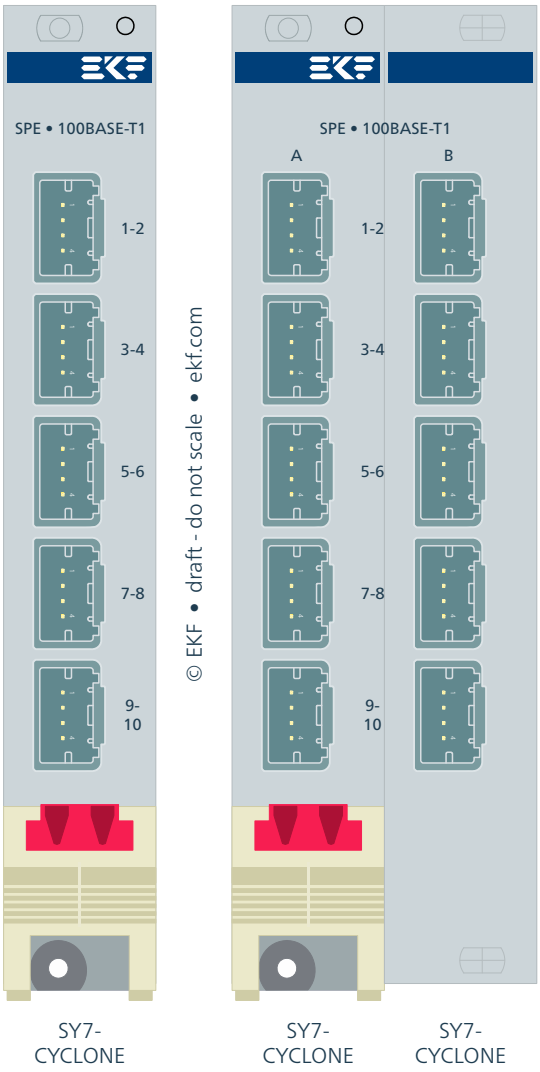
Regulatory

- Long term availability
- Designed & manufactured in Germany
- ISO 9001 certified quality management
- Rugged solution (coating, sealing, underfilling on request)
- RoHS compliant
- Industrial operation temperature range -40°C to +85°C
- Humidity 5% ... 95% RH non condensing
- Altitude -300m ... +3000m
- Shock 15g 0.33ms, 6g 6ms
- Vibration 1g 5-2000Hz
- MTBF tbd years
- EC Regulations EN55022, EN55024, EN60950-1 (UL60950-1/IEC60950-1)

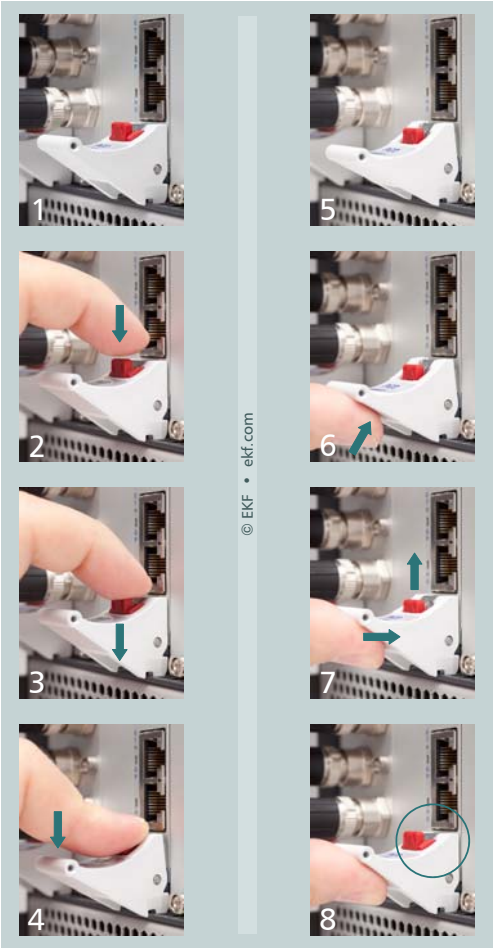
Block Diagram



Front Panel


SPE • 100BASE-T1
1-2
3-4
5-6
7-8
9-10
© EKF • draft - do not scale • ekf.com
SPE • 100BASE-T1
A
B
1-2
3-4
5-6
7-8
9-10
SY7-CYCLONE
SY7-CYCLONE
SY7-CYCLONE

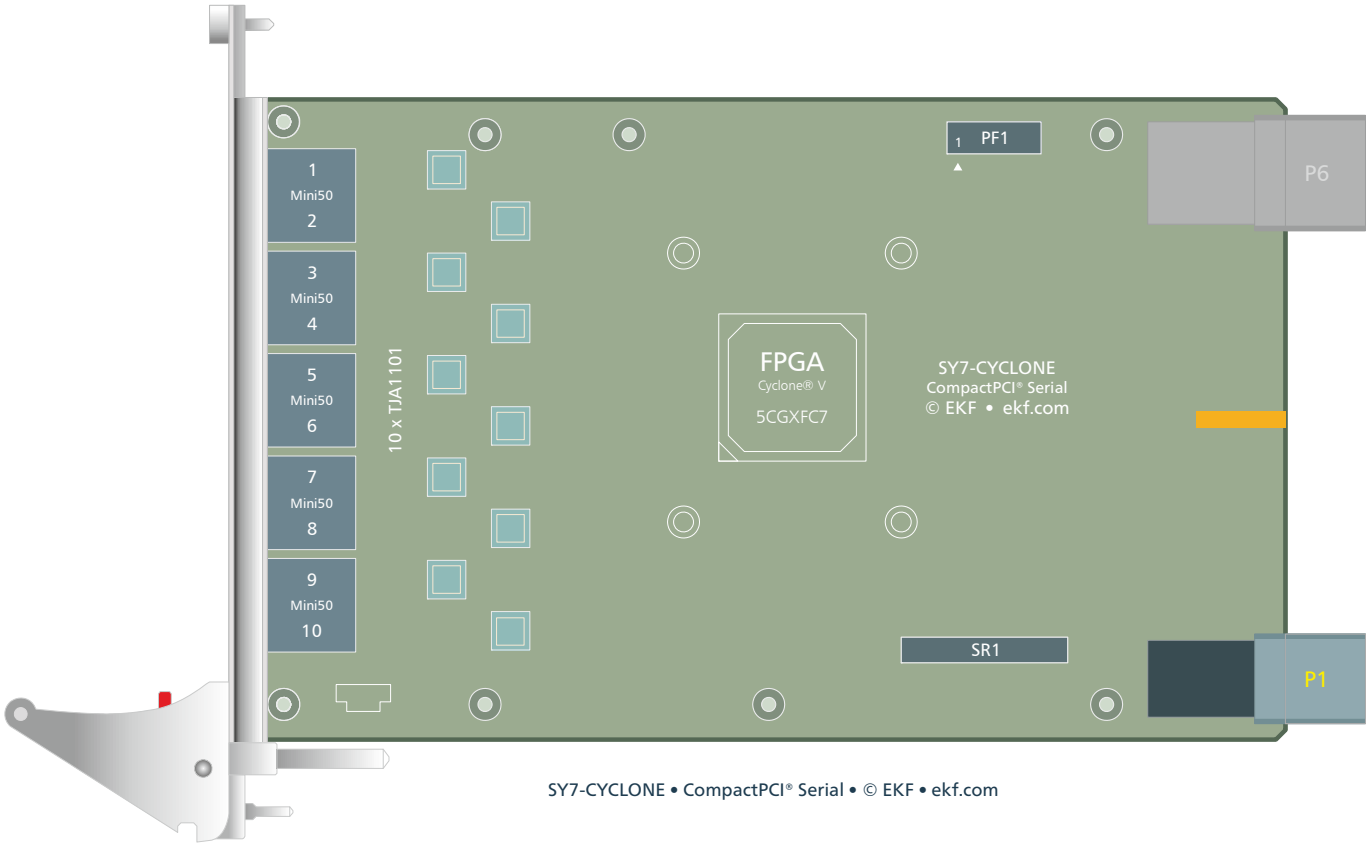
Please note: The front handle is provided with a built-in microswitch, which is used to disable the on-board power circuit when released. Vice versa, the *on-board devices are enabled not before the handle gets locked*. Please refer to the illustration below and make sure that the eject lever has reached its final position for proper board operation, as shown in picture 8. A gentle click should be audible, when the red actuator pin moves into its raised position, indicating that the board is locked and ready for use.



1 - 4: remove board
5 - 8: install board

1 & 8: on-board power enabled
2-7: on-board power disabled

Component Assembly



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FPGA

The SY7-CYCLONE is a universal hardware platform for FPGA based industrial networking and was designed for proprietary applications, to be specified by the customer.

The SY7-CYCLONE is equipped with a CYCLONE® V FPGA (Altera/Intel®). The board is normally populated with a 5CGXFC7C6F23I7N. There are several programmable interface blocks wired from the FPGA to on-board connectors and components:

- PCI Express® (hard IP), four lanes tied to the CompactPCI® Serial backplane connector P1 for host communication with the CPU system slot card
- 10 x automotive Single Pair Ethernet PHYs (100BASE-T1)
- Option interface connector SR1 for versatile mezzanine expansion
- Memory interfaces to DDR3L RAM and I2C NV storage devices (2 x EEPROM)
- JTAG connector PF1

A complete SY7-CYCLONE FPGA reference design for the Intel® Quartus® Prime suite is available, as a starting point for custom specific application programming, and in addition a Linux based test tool.

FPGA Default Signal Usage

Name	Bk	Pin	Type
PE_CLKIN+		V4	I
PE_CLKIN-		U4	I
1_PE_TX00+		Y4	O
1_PE_TX00-		Y3	O
1_PE_RX00+		AA2	I
1_PE_RX00-		AA1	I
1_PE_TX01+		U2	O
1_PE_TX00-		U1	O
1_PE_RX01+		W2	I
1_PE_RX01-		W1	I
1_PE_TX02+		N2	O
1_PE_TX02-		N1	O
1_PE_RX02+		R2	I
1_PE_RX02-		R1	I
1_PE_TX03+		J2	O
1_PE_TX03-		J1	O
1_PE_RX03+		L2	I
1_PE_RX03-		L1	I
PHY1_TX_EN	5	T20	O
PHY1_TXD1	5	T22	O
PHY1_TXD0	5	R21	O
PHY1_MDIO	5	P19	I/O
PHY1_MDC	5	N19	O
PHY1_RXD1	5	N20	I
PHY1_RXD0	5	N20	I
PHY1_CRSDV	5	N21	I
PHY1_REFCLK	5	M21	O
PHY1_ RST#	5	L19	O
FPGA_PHY1_EN	8	H9	O
PHY2_TX_EN	5	M22	O
PHY2_TXD1	7	D21	O
PHY2_TXD0	5	K21	O
PHY2_MDIO	7	J22	I/O
PHY2_MDC	7	J21	O
PHY2_RXD1	7	H21	I
PHY2_RXD0	7	G22	I
PHY2_CRSDV	7	F22	I
PHY2_REFCLK	7	G21	O

Name	Bk	Pin	Type
PHY2_RST#	7	E22	O
FPGA_PHY2_EN	7	H10	O
PHY3_TX_EN	7	E21	O
PHY3_TXD1	7	D22	O
PHY3_TXD0	7	A20	O
PHY3_MDIO	7	C21	I/O
PHY3_MDC	7	B21	O
PHY3_RXD1	7	B22	I
PHY3_RXD0	7	E20	I
PHY3_CRSDV	7	B20	I
PHY3_REFCLK	7	A22	O
PHY3_RST#	7	C20	O
FPGA_PHY3_EN	7	J11	O
PHY4_TX_EN	7	F20	O
PHY4_TXD1	7	E19	O
PHY4_TXD0	7	F19	O
PHY4_MDIO	7	G20	I/O
PHY4_MDC	7	H20	O
PHY4_RXD1	7	K20	I
PHY4_RXD0	7	D19	I
PHY4_CRSDV	7	J19	I
PHY4_REFCLK	7	C19	O
PHY4_RST#	7	A19	O
FPGA_PHY4_EN	8	G6	O
PHY5_TX_EN	7	C18	O
PHY5_TXD1	7	B18	O
PHY5_TXD0	7	A18	O
PHY5_MDIO	7	J18	I/O
PHY5_MDC	7	H18	O
PHY5_RXD1	7	G18	I
PHY5_RXD0	7	F18	I
PHY5_CRSDV	7	D17	I
PHY5_REFCLK	7	B17	O
PHY5_ RST#	7	A17	O
FPGA_PHY5_EN	8	G8	O
PHY6_TX_EN	7	J17	O
PHY6_TXD1	7	G17	O
PHY6_TXD0	7	B16	O

Name	Bk	Pin	Type
PHY6_MDIO	7	C16	I/O
PHY6_MDC	7	E16	O
PHY6_RXD1	7	E15	I
PHY6_RXD0	7	E14	I
PHY6_CRSDV	7	C15	I
PHY6_REFCLK	7	B15	O
PHY6_ RST#	7	A15	O
FPGA_PHY6_EN	8	F7	O
PHY7_TX_EN	7	D13	O
PHY7_TXD1	7	C13	O
PHY7_TXD0	7	B13	O
PHY7_MDIO	7	A13	I/O
PHY7_MDC	7	B12	O
PHY7_RXD1	7	A12	I
PHY7_RXD0	7	C11	I
PHY7_CRSDV	7	B11	I
PHY7_REFCLK	8	A10	O
PHY7_ RST#	8	B10	O
FPGA_PHY7_EN	7	G11	O
PHY8_TX_EN	7	F15	O
PHY8_TXD1	7	G15	O
PHY8_TXD0	7	H15	O
PHY8_MDIO	7	G16	I/O
PHY8_MDC	7	H16	O
PHY8_RXD1	7	K16	I
PHY8_RXD0	5	M16	I
PHY8_CRSDV	5	K17	I
PHY8_REFCLK	5	L17	O
PHY8_ RST#	7	F14	O
FPGA_PHY8_EN	7	G12	O
PHY9_TX_EN	8	C9	O
PHY9_TXD1	8	A9	O
PHY9_TXD0	8	A8	O
PHY9_MDIO	8	C8	I/O
PHY9_MDC	8	A7	O
PHY9_RXD1	8	B7	I
PHY9_RXD0	8	B6	I
PHY9_CRSDV	8	A5	I

FPGA Default Signal Usage

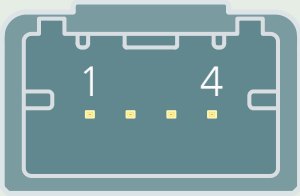
Name	Bk	Pin	Type
PHY9_REFCLK	8	C6	O
PHY9_RST#	8	B5	O
FPGA_PHY9_EN	8	E7	O
PHY10_TX_EN	7	D12	O
PHY10_TXD1	7	E12	O
PHY10_TXD0	7	F13	O
PHY10_MDIO	7	G13	I/O
PHY10_MDC	7	H13	O
PHY10_RXD1	7	J13	I
PHY10_RXD0	8	E10	I
PHY10_CRSDV	8	F10	I
PHY10_REFCLK	8	F9	O
PHY10_ RST#	8	G10	O
FPGA_PHY10_EN	8	D6	O
INTBRD0	3A	R5	I/O
INTBRD1	3A	V6	I/O
INTBRD2	3A	U6	I/O
INTBRD3	3A	R6	I/O
INTBRD4	3A	N6	I/O
INTBRD5	3A	M6	I/O
INTBRD6	3A	U7	I/O
INTBRD7	3A	T7	I/O
INTBRD8	3A	R7	I/O
INTBRD9	3A	P7	I/O
INTBRD10	3A	M7	I/O
INTBRD11	3A	W8	I/O
INTBRD12	3A	U8	I/O
INTBRD13	3A	W9	I/O
INTBRD14	8	L7	I/O
INTBRD15	7	L8	I/O
INTBRD16	8	K7	I/O
INTBRD17	7	K9	I/O
INTBRD18	8	J8	I/O
INTBRD19	8	J9	I/O
FPGA_SENS	8	H6	I
HEALTH_IN	8	H8	I
CRC_ERROR	5	T17	O
BROWN_OUT	8	J7	I
TEMP_SDA	5	K22	I/O
TEMP_SCL	5	L22	O

Name	Bk	Pin	Type
CLK50	5	N16	I
CLK100	3A	T8	I
MEM_RST#	4	W21	O
MEM_CK	3B	U12	O
MEM_CK#	3B	U11	O
MEM_ODT	4	AA13	O
MEM_CS#	3B	N8	O
MEM_CKE	4	AA19	O
MEM_A0	3B	AA12	O
MEM_A1	3B	Y11	O
MEM_A2	3B	AB11	O
MEM_A3	3B	AB10	O
MEM_A4	3B	R11	O
MEM_A5	3B	R10	O
MEM_A6	3B	P12	O
MEM_A7	3B	R12	O
MEM_A8	3B	U10	O
MEM_A9	3B	T9	O
MEM_A10	3B	AB8	O
MEM_A11	3B	AA8	O
MEM_A12	3B	AB7	O
MEM_A13	3B	AA7	O
MEM_A14	3B	V10	O
MEM_A15	3B	V9	O
MEM_BA0	3B	Y9	O
MEM_BA1	3B	R9	O
MEM_BA2	3B	T10	O
MEM_RAS#	3B	AA10	O
MEM_CAS#	3B	AA9	O
MEM_WE#	3B	AB5	O
MEM_DQ0	4	V13	I/O
MEM_DQ1	4	U13	I/O
MEM_DQ2	4	AB12	I/O
MEM_DQ3	4	AA14	I/O
MEM_DQ4	4	Y14	I/O
MEM_DQ5	4	Y15	I/O
MEM_DQ6	4	AA15	I/O
MEM_DQ7	4	AB17	I/O
MEM_DQS	4	T13	I/O
MEM_DQS#	4	T12	I/O

Name	Bk	Pin	Type
EEP_SCL	5	P16	O
EEP_SDA	5	R16	I/O
USR_EEP_SCL	5	T15	O
USR_EEP_SDA	5	R15	I/O

Front Panel Connectors

The SY7-CYCLONE is provided with five Mini50 front panel headers (Molex 4 circuit USCAR approved). Each connector is used for two independent Ethernet ports according to IEEE 802.3bw 100BASASE-T1, hence a total of 10 ports is available from the front, for attachment of suitable cable connectors.

5 x Front Panel Connectors Mini50 #279.01.04.00 Molex Part 34793		
	1	TRXP (PHY1 PHY3 PHY5 PHY7 PHY9)
	2	TRXM (PHY1 PHY3 PHY5 PHY7 PHY9)
	3	TRXP (PHY2 PHY4 PHY6 PHY8 PHY10)
	4	TRXM (PHY2 PHY4 PHY6 PHY8 PHY10)

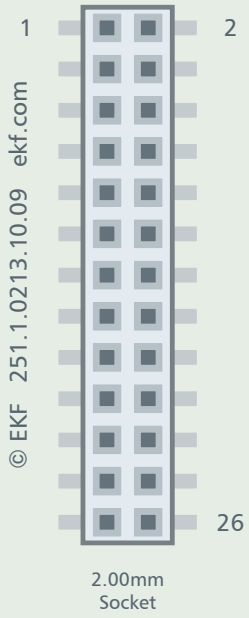
Suitable cable connectors are Molex 347910040 receptacles, to be combined with crimp terminals Molex 5600230421 or 5600230444.

Mezzanine Connector SR1 (Option)

As an option, the SY7-CYCLONE can be expanded by a mezzanine module, intended for a secondary FPGA. The FPGA module fits on the connector SR1, with a suggested mechanical pitch of 4HP (8HP front panel assembly in total for the SY7-CYCLONE base card and the mezzanine module). The mezzanine board may be custom specific, but also a second SY7-CYCLONE card can be coupled this way for immediate data exchange between both FPGAs.

As an alternate, the connector SR1may be used for test and debug, or custom specific I/O.

SR1 • Mezzanine Expansion Interface
2.00mm Socket 2 x 22 (251.1.0213.10.09)



INTBRD0	1	2	INTBRD1
INTBRD2	3	4	INTBRD3
INTBRD4	5	6	INTBRD5
INTBRD6	7	8	INTBRD7
INTBRD8	9	10	INTBRD9
INTBRD10	11	12	INTBRD11
INTBRD12	13	14	INTBRD13
INTBRD14	15	16	INTBRD15
INTBRD16	17	18	INTBRD17
INTBRD18	19	20	INTBRD19
GND	21	22	GND
HOTSWP	23	24	HEALTH_OUT
BROWN_OUT	25	26	HEALTH_IN

HEALTH_IN/HEALTH_OUT role swapped on mezzanine SY7-CYCLONE card

JTAG Connector PF1

The SY7-CYCLONE is equipped with a 2x5 pos. female side entry connector (e.g. Tyco Micro-Match 1-215460-0 or Würth 690368171072 WR-MM MiniModule) for JTAG attachment via 1.27mm micro ribbon flat cable assembly.

PF1 • FPGA JTAG Female Side Entry Connector (241.4.0205.10.01)			
TCK	1		
		2	GND
TDO	3		
		4	+3.3V
TMS	5		
		6	
	7		
		8	
TDI	9		
		10	GND

P1 CompactPCI® Serial Backplane Connector

P1 CompactPCI® Serial Peripheral Slot Backplane Connector EKF Part #250.3.1206.20.02 • 72 pos. 12x6, 14mm Width												
P1	A	B	C	D	E	F	G	H	I	J	K	L
6	GND	1 PE TX02+	1 PE TX02-	GND	1 PE RX02+	1 PE RX02-	GND	1 PE TX03+	1 PE TX03-	GND	1 PE RX03+	1 PE RX03-
5	1 PE TX00+	1 PE TX00-	GND	1 PE RX00+	1 PE RX00-	GND	1 PE TX01+	1 PE TX01-	GND	1 PE RX01+	1 PE RX01-	GND
4	GND	*1_ USB2+*	*1_ USB2-*	GND	PE_CLK IN+	PE_CLK IN-	GND	*1 SATA TX+*	*1 SATA TX-*	GND	*1 SATA RX+*	*1 SATA RX-*
3	*1 USB3 TX+*	*1 USB3 TX-*	GA0	*1 USB3 RX+*	*1 USB3 RX-*	GA1	*SATA SDI*	*SATA SDO*	GA2	*SATA SCL*	*SATA SL*	GA3
2	GND	I2C SCL	I2C SDA	GND	*RSV*	*RSV*	GND	RST#	WAKE#	GND	PE_ EN#	SYS EN#
1	+12V	STBY	GND	+12V	+12V	GND	+12V	+12V	GND	+12V	+12V	GND

pin positions printed white/italic: not connected

For signal descriptions please refer to PICMG CPCI-S.0 R1.0 CompactPCI® Serial Specification

Reference Documents		
Term	Document	Origin
CompactPCI® Serial	CPCI-S.0	www.picmg.org
CYCLONE® V	Intel® Cyclone V Device Datasheet CV-51002 and other design resources	www.altera.com

Ordering Information
For popular SY7-CYCLONE SKUs please refer to www.ekf.com/liste/liste_21.html#SY7

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